



孕龍科技股份有限公司
ZEROPLUS TECHNOLOGY CO.,LTD

Instrument Business Department

ARITHMETICAL LOGIC Specification

Version : V1.00

Content

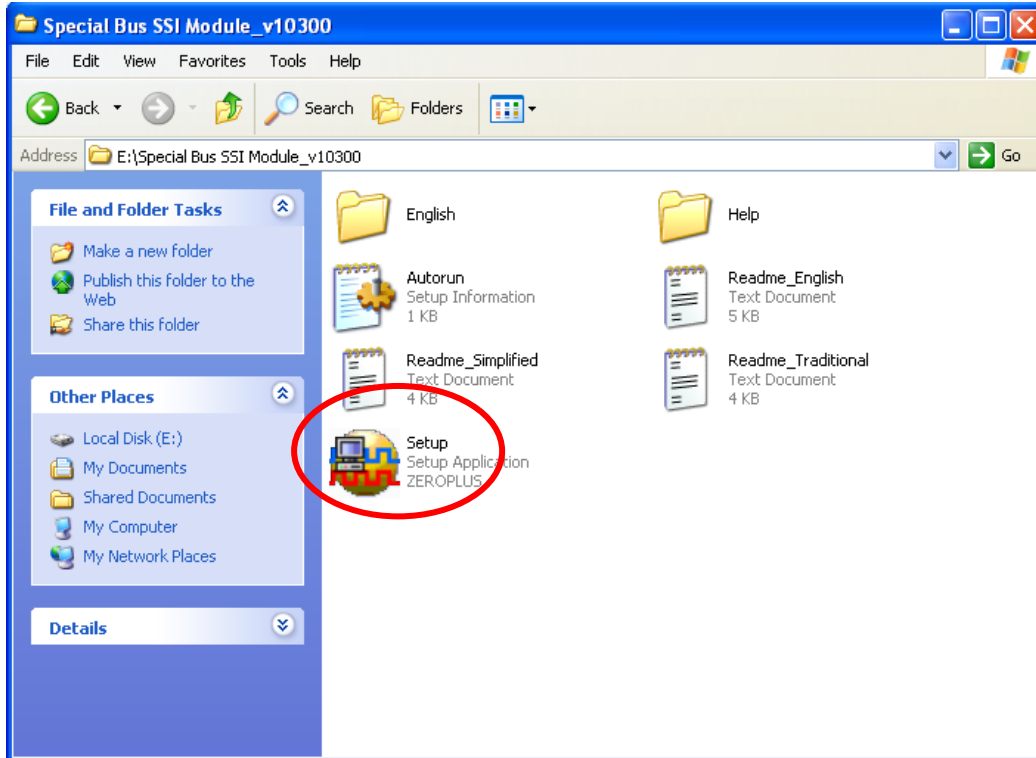
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1 Software Installation

Please install the software as the following steps :

※ Remark: The installation steps for all buses are the same; you can complete installation by following procedures. The below is an example to install SSI bus.

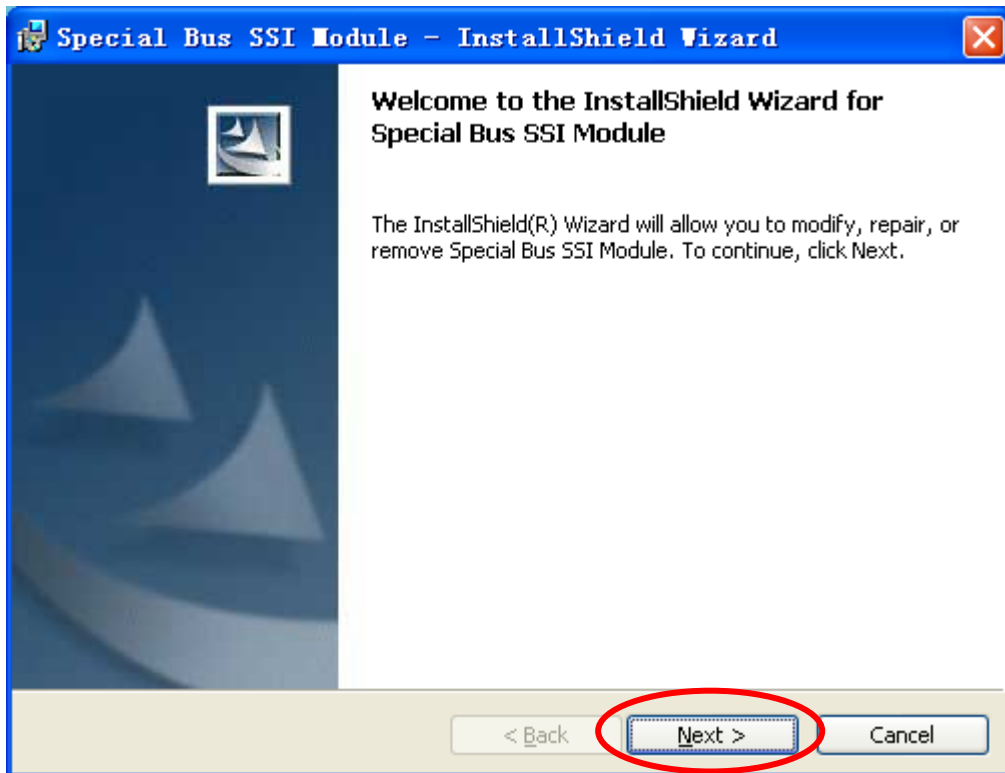
STEP 1. Install Bus Module



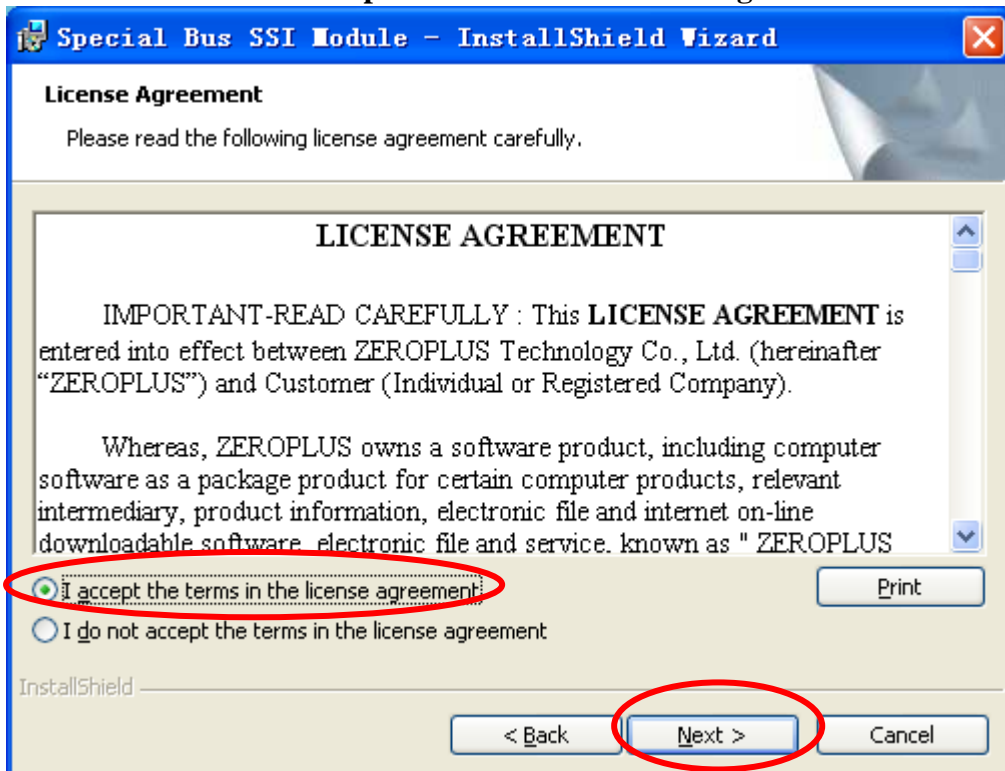
STEP 2. Click Install.



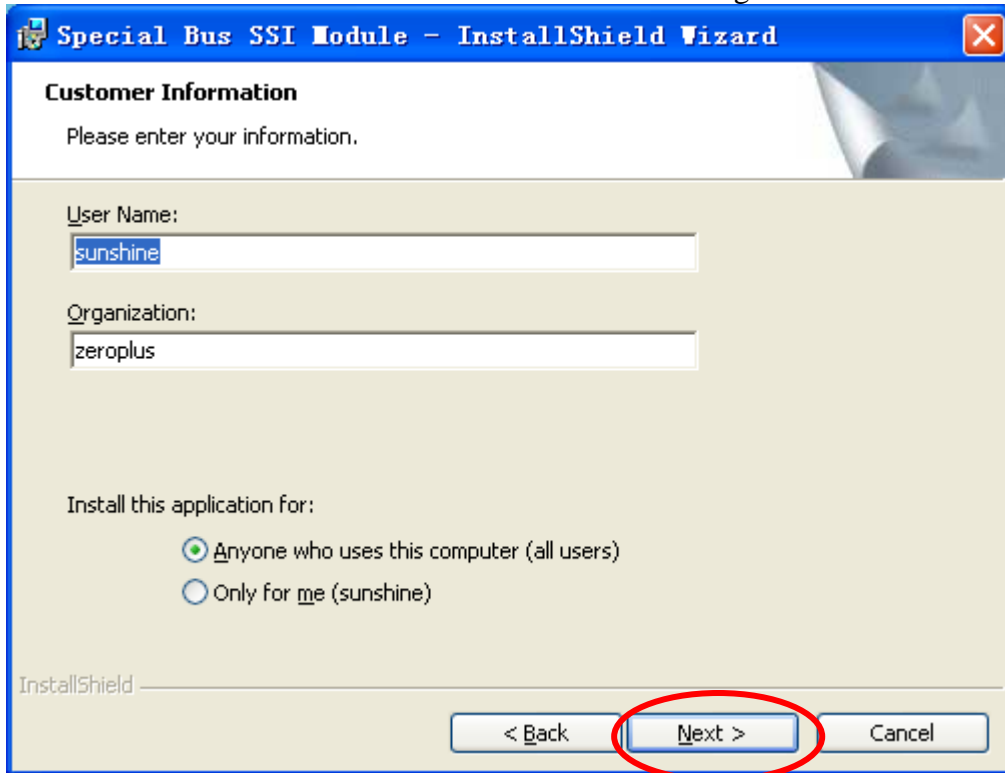
STEP 3. Click Next.



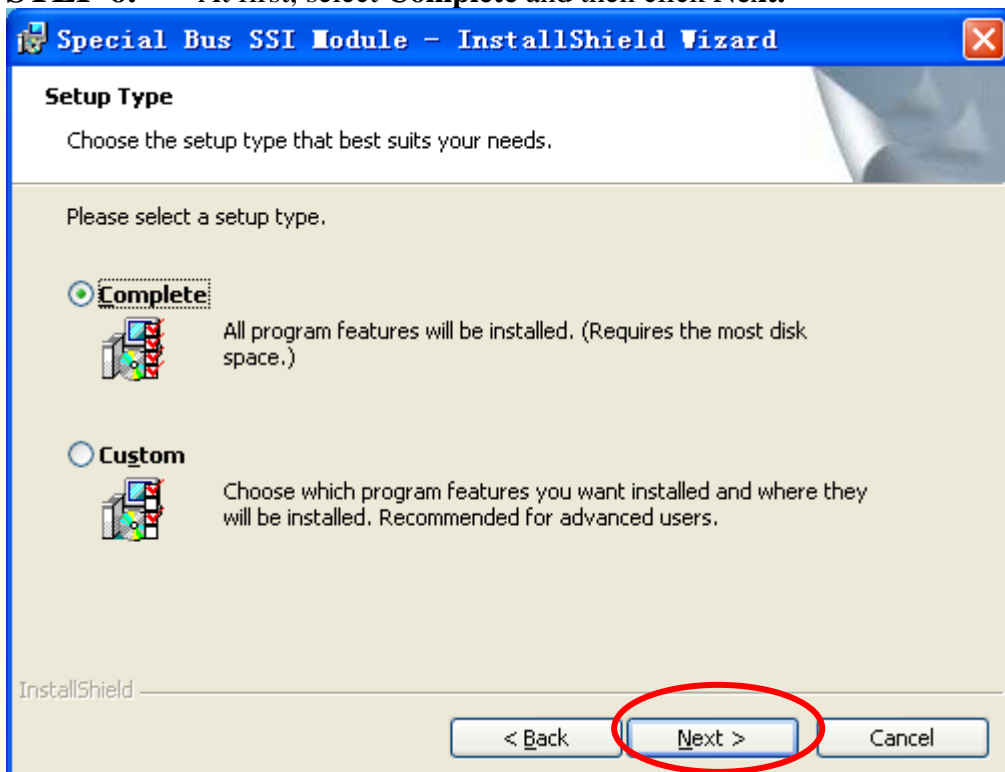
STEP 4. Select **I accept the terms in the license agreement**, and then press Next.



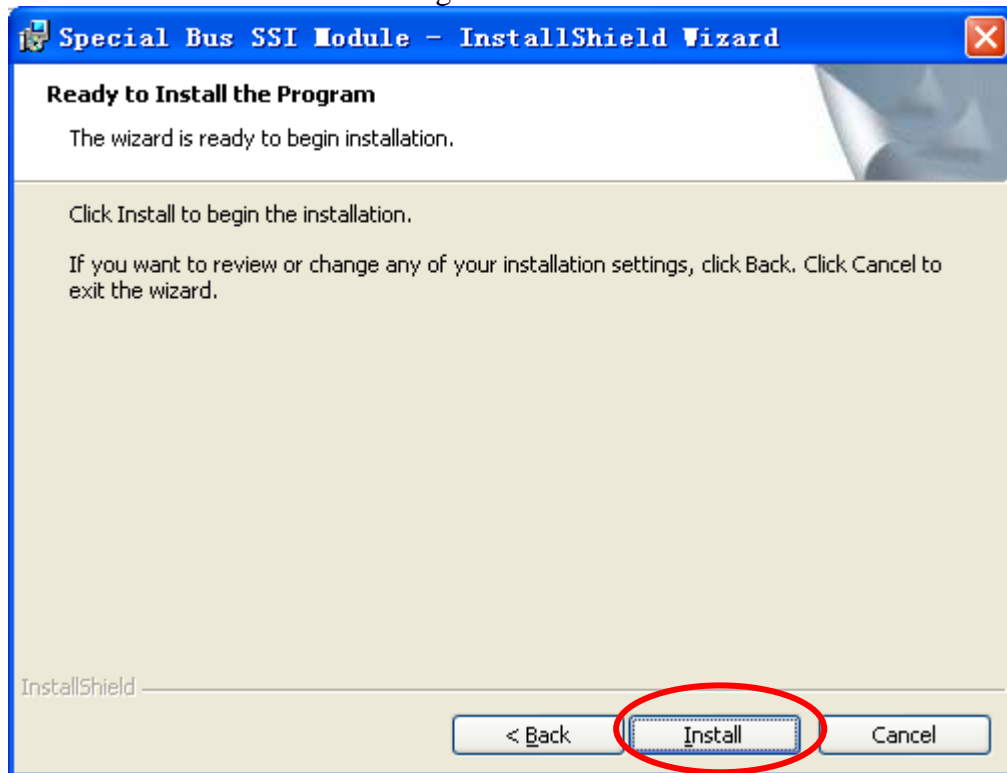
STEP 5. Fill in user information in the below dialog box and click **Next**.



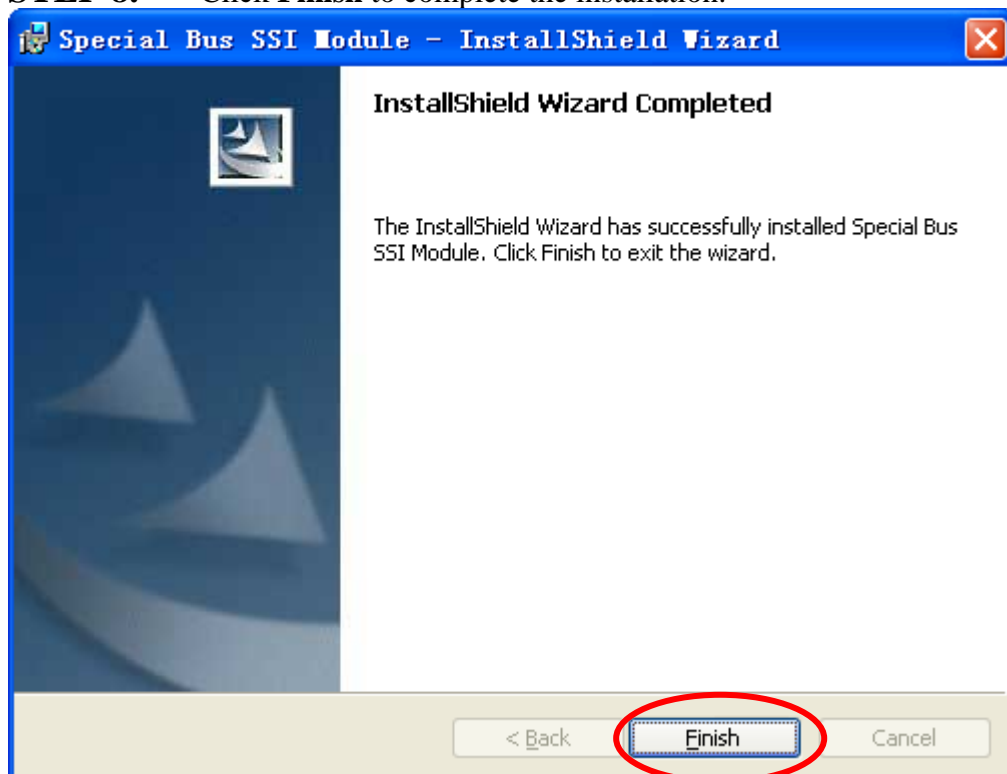
STEP 6. At first, select **Complete** and then click **Next**.



STEP 7. Click **Install** to begin the installation.

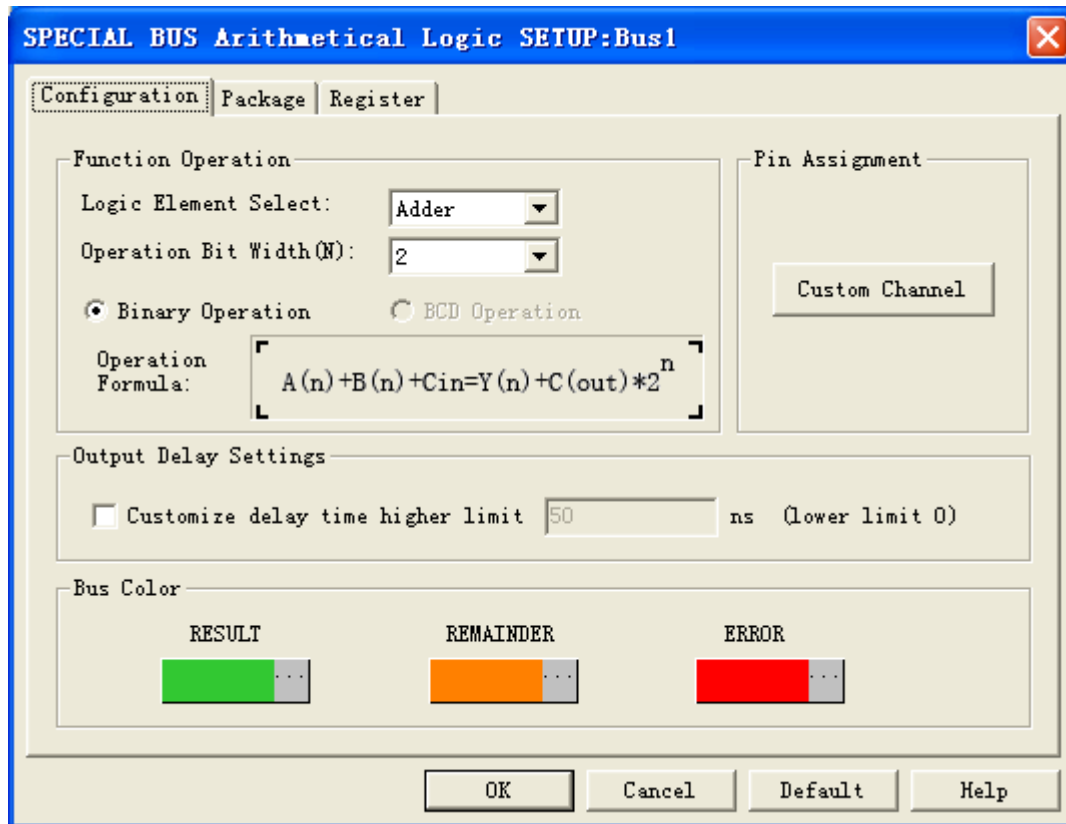


STEP 8. Click **Finish** to complete the installation.

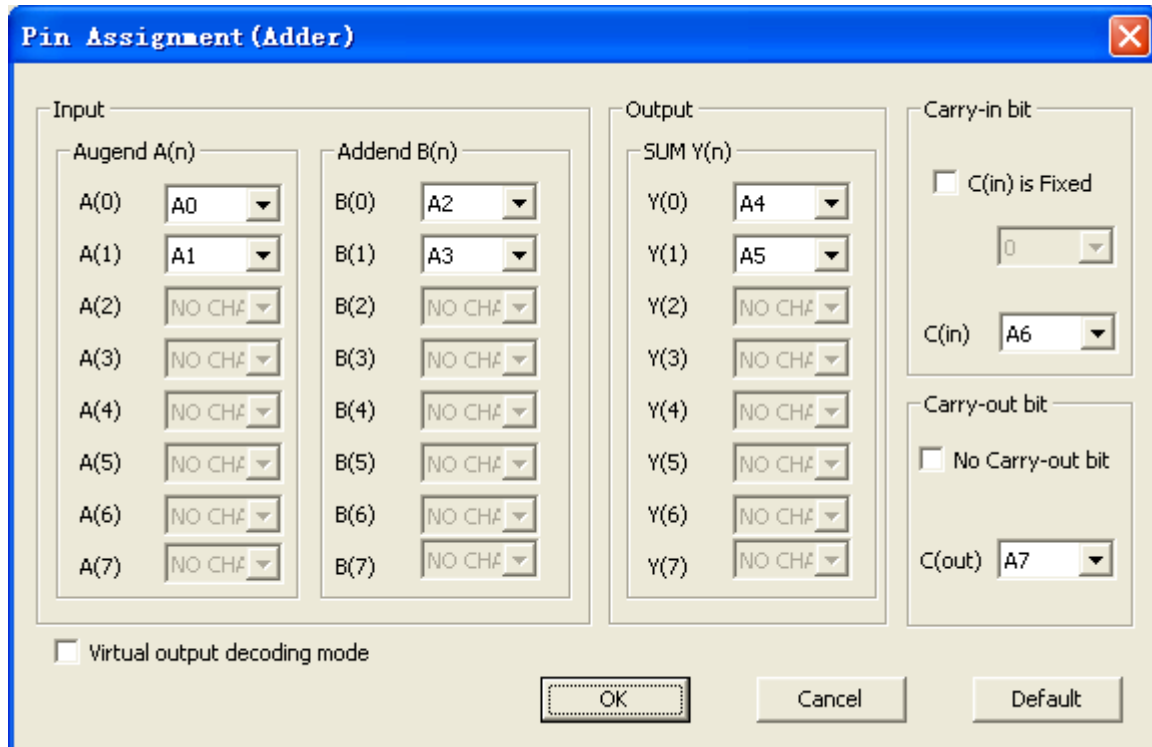


2 User Interface

Please refer to the below images to select options of setting Arithmetical Logic module



Custom Channel: Adder



Custom Channel: Subtract

Pin Assignment (Subtract)

Input		Output	
Minuend A(n)	Subtrahend B(n)	Difference Y(n)	
A(0) A0	B(0) A2	Y(0) A4	Borrow Input
A(1) A1	B(1) A3	Y(1) A5	<input type="checkbox"/> C(in) is Fixed
A(2) NO CH#	B(2) NO CH#	Y(2) NO CH#	0
A(3) NO CH#	B(3) NO CH#	Y(3) NO CH#	C(in) A6
A(4) NO CH#	B(4) NO CH#	Y(4) NO CH#	Borrow Output
A(5) NO CH#	B(5) NO CH#	Y(5) NO CH#	<input type="checkbox"/> No Borrow Output
A(6) NO CH#	B(6) NO CH#	Y(6) NO CH#	C(out) A7
A(7) NO CH#	B(7) NO CH#	Y(7) NO CH#	

Virtual output decoding mode

OK Cancel Default

Custom Channel: Multiplier

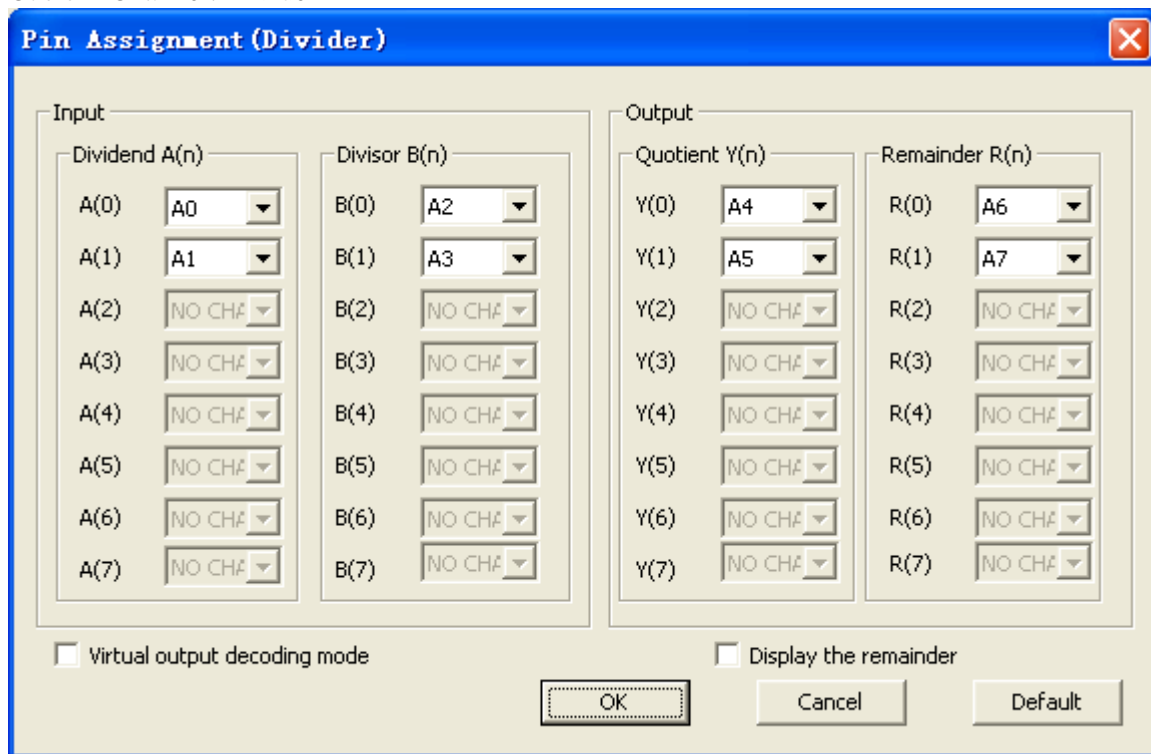
Pin Assignment (Multiplier)

Input		Output	
Multiplicand A(n)	Multiplicator B(n)	Product Y(2n)	
A(0) A0	B(0) A2	Y(0) A4	Y(8) NO CH#
A(1) A1	B(1) A3	Y(1) A5	Y(9) NO CH#
A(2) NO CH#	B(2) NO CH#	Y(2) A6	Y(10) NO CH#
A(3) NO CH#	B(3) NO CH#	Y(3) A7	Y(11) NO CH#
A(4) NO CH#	B(4) NO CH#	Y(4) NO CH#	Y(12) NO CH#
A(5) NO CH#	B(5) NO CH#	Y(5) NO CH#	Y(13) NO CH#
A(6) NO CH#	B(6) NO CH#	Y(6) NO CH#	Y(14) NO CH#
A(7) NO CH#	B(7) NO CH#	Y(7) NO CH#	Y(15) NO CH#

Virtual output decoding mode

OK Cancel Default

Custom Channel: Divider



Function Operation settings:

Logic Element Select: User can select the arithmetical element as his/her requirements from the dropdown menu; the options are Adder, Subtract, Multiplier and Divider.

Operation Bit Width Option: The Bit Width can be selected from the dropdown menu; the different options are 2, 4 and 8.

Select the Binary Operation or BCD Operation (The BCD operation is available for the bit width is not less than 4 bit.)

Pin Assignment:

Custom Channel Option: When user selects the different arithmetical elements, the corresponding arithmetical element channel setting will present, and user should set the required channels and the number of the channels.

Output Delay Settings:

Customize the delay time: The default of the delay time higher limit is 50ns and the max. higher limit is 5000ns.

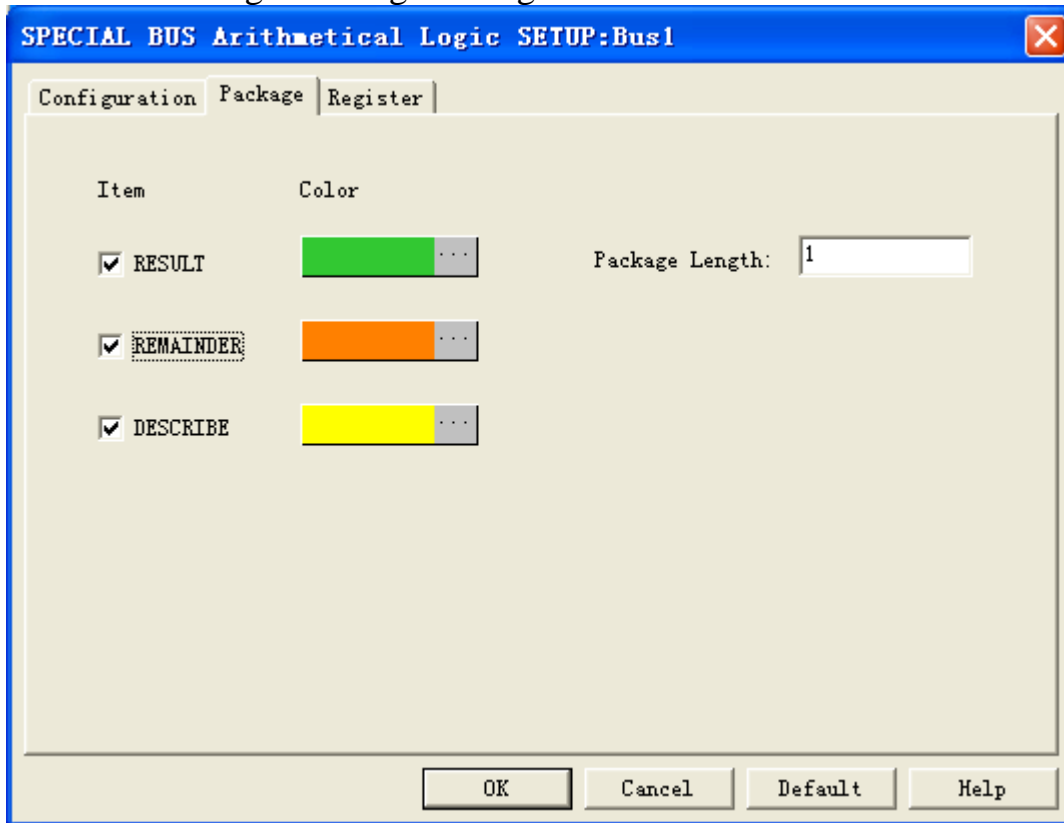
Bus Color

User can customize the color.

Virtual output decoding mode:

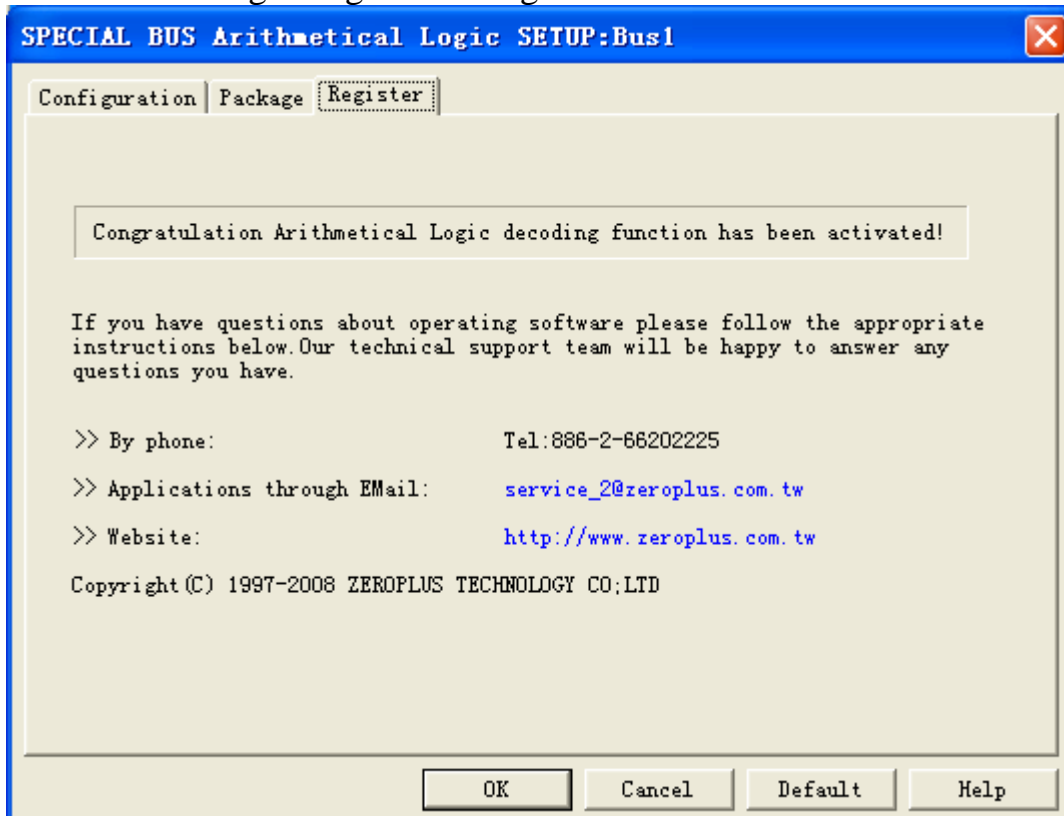
User can set the virtual output decoding mode under every channel of Pin Assignment, when it is selected, the output channel is disabled.

Arithmetical Logic Package Dialog Box



In the package part, user can vary the displaying item and the package color and set the package length.

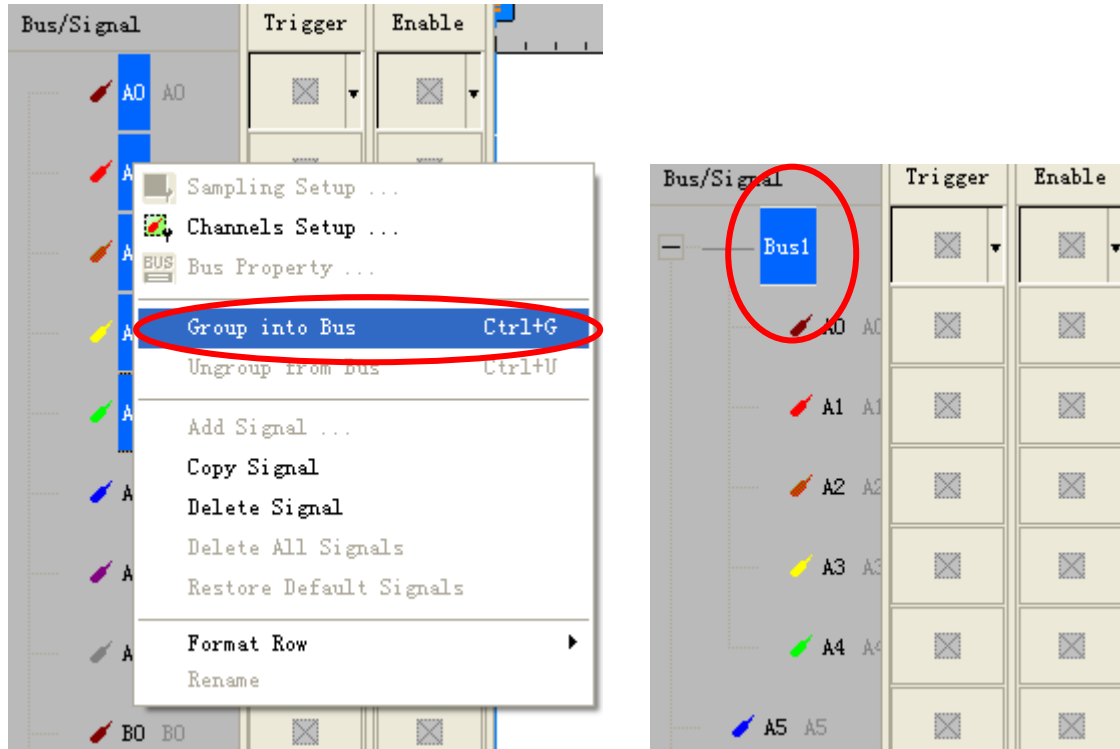
Arithmetical Logic Register Dialog Box



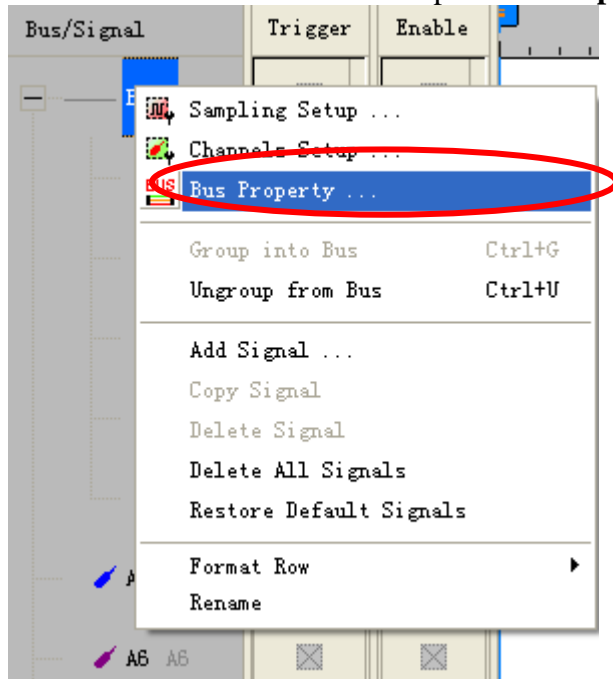
There is ZeroPlus company information. If you have any questions about software operations, you can contact ZeroPlus by Telephone or Email.

3 Operating Instructions

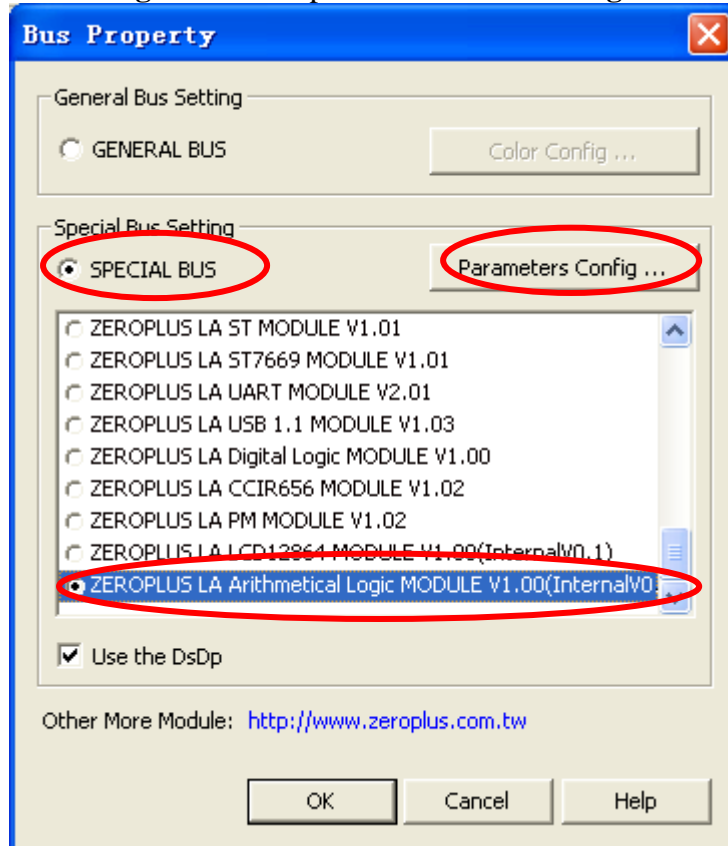
STEP 1. At first, group the unanalyzed channels into **bus1** by pressing the **Right Key** on mouse.



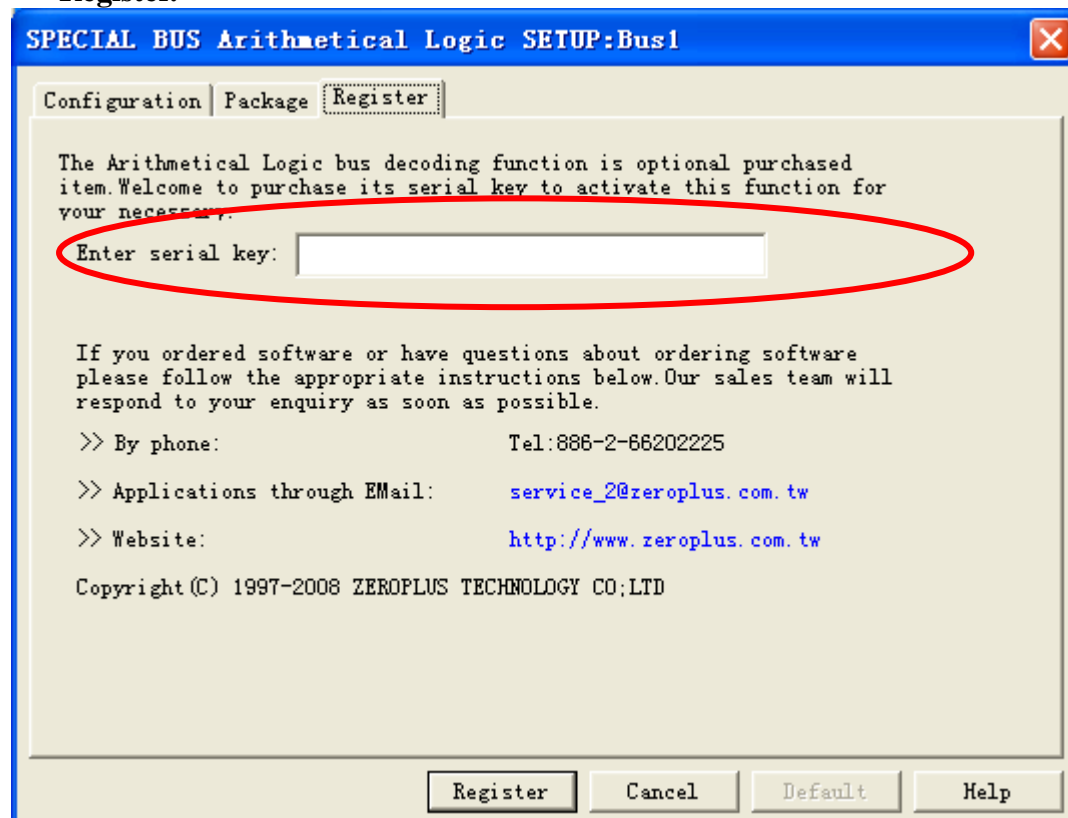
STEP 2. Select **Bus1**, then press **Right key** on mouse to list menu, then press **Bus Property** or **Bus bar** on the toolbar to open **Bus Property** dialog box.



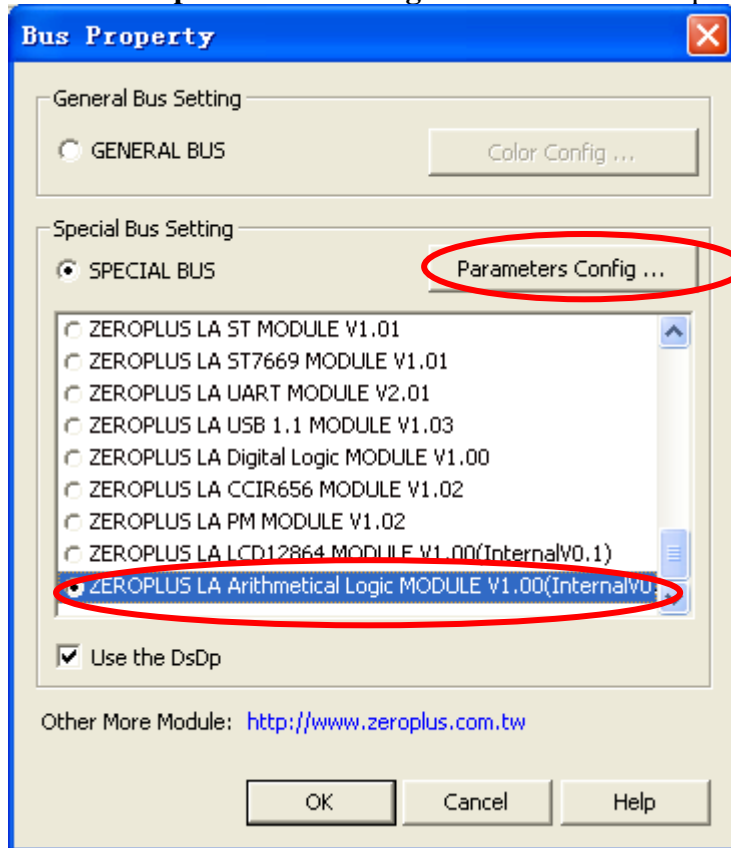
STEP 3. For Special Bus Arithmetical Logic Parameters Configuration, select Special Bus, and then choose **ZEROPLUS Arithmetical Logic MODULE V1.00**, next click **Parameters Configuration** to open **Parameters Configuration** dialog box.



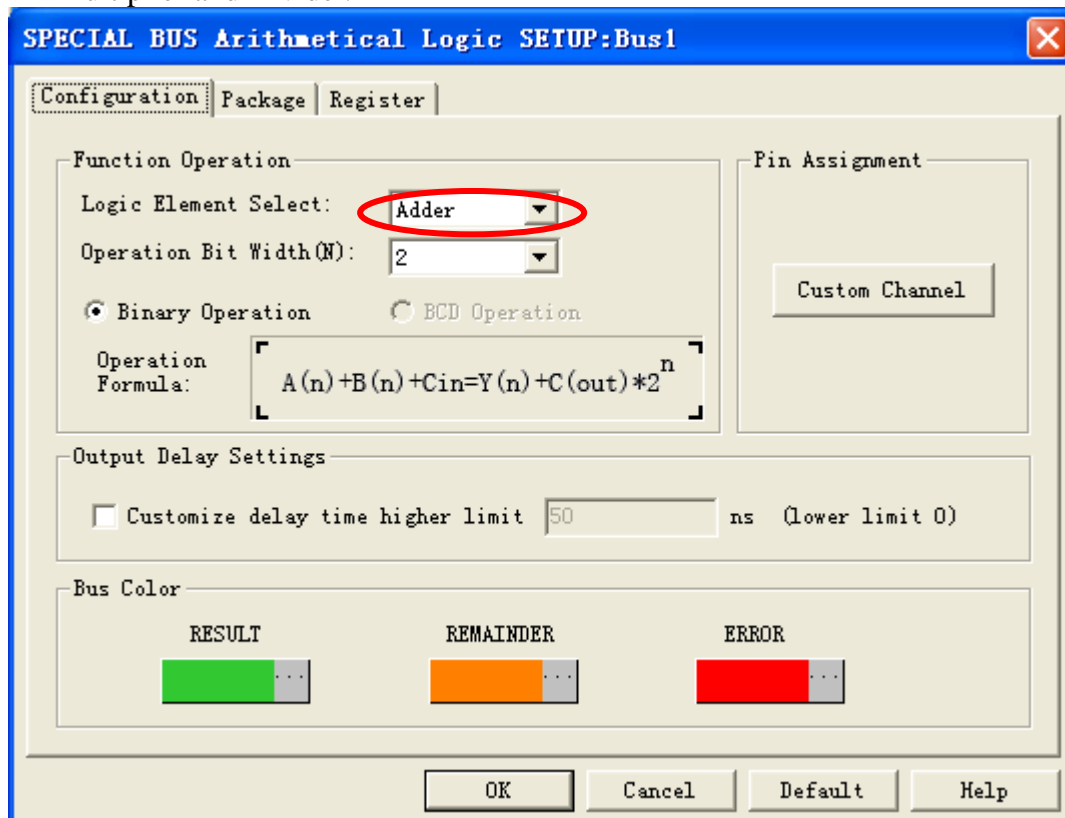
STEP 4. Press Register tab to type the serial key number of logic analyzer. Then, press **Register**.



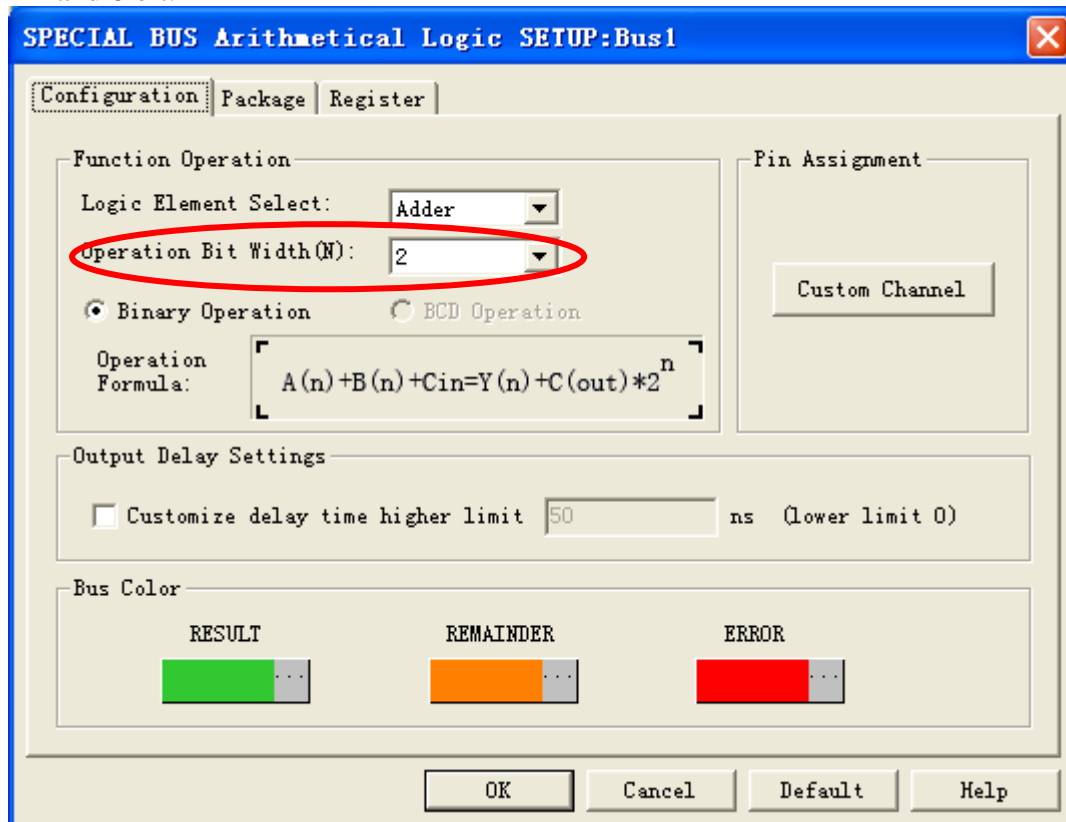
STEP 5. After completing **Register**, come back to the **Bus property** dialog box, and then click the **parameters configuration** to start the Special Bus Digital Logic setup.



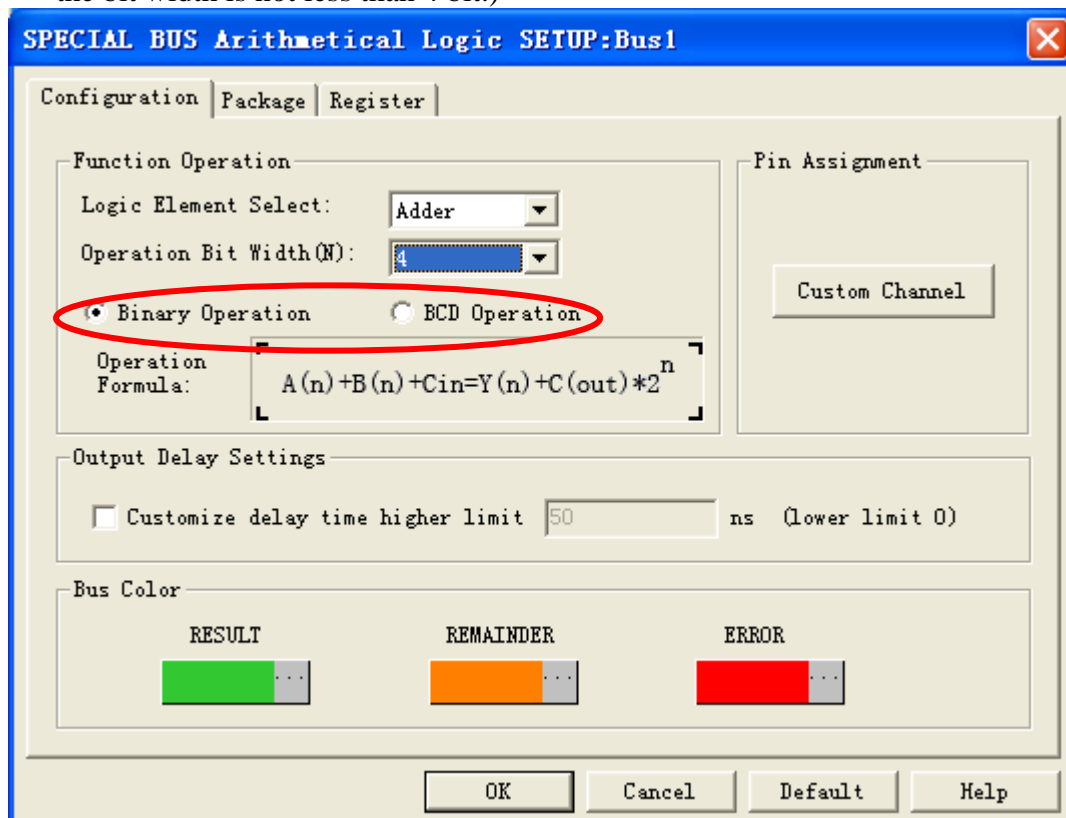
STEP 6. Arithmetical operation settings, the useable logic elements are Adder, Subtract, Multiplier and Divider.



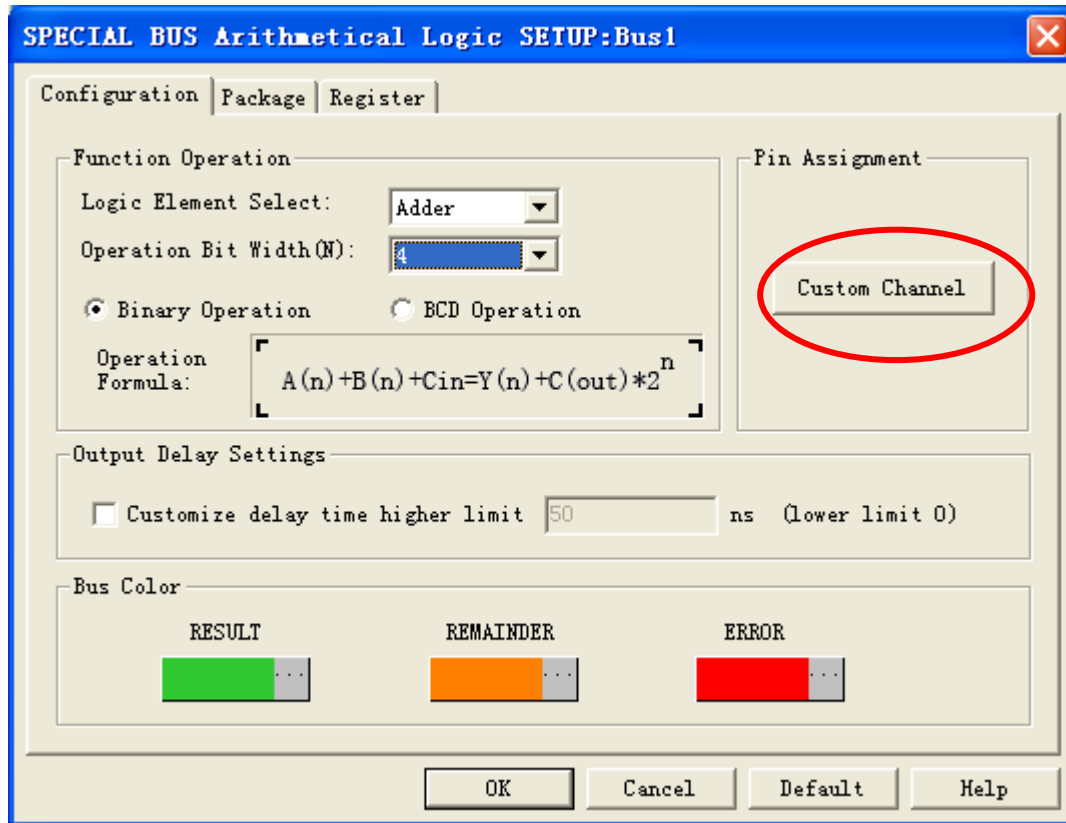
STEP 7. The Operation Bit Width can be selected from the three options, there are: 2 bit, 4 bit and 8 bit.



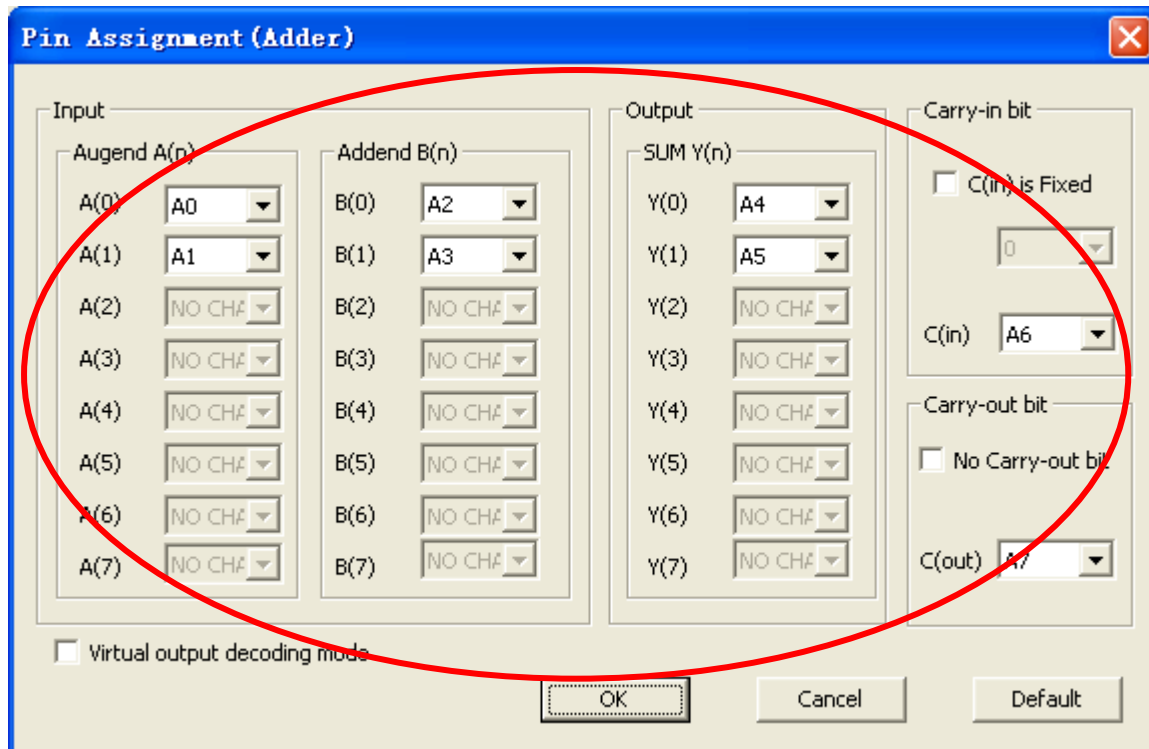
STEP 8. Select the Binary Operation or BCD Operation (The BCD operation is available for the bit width is not less than 4 bit.)



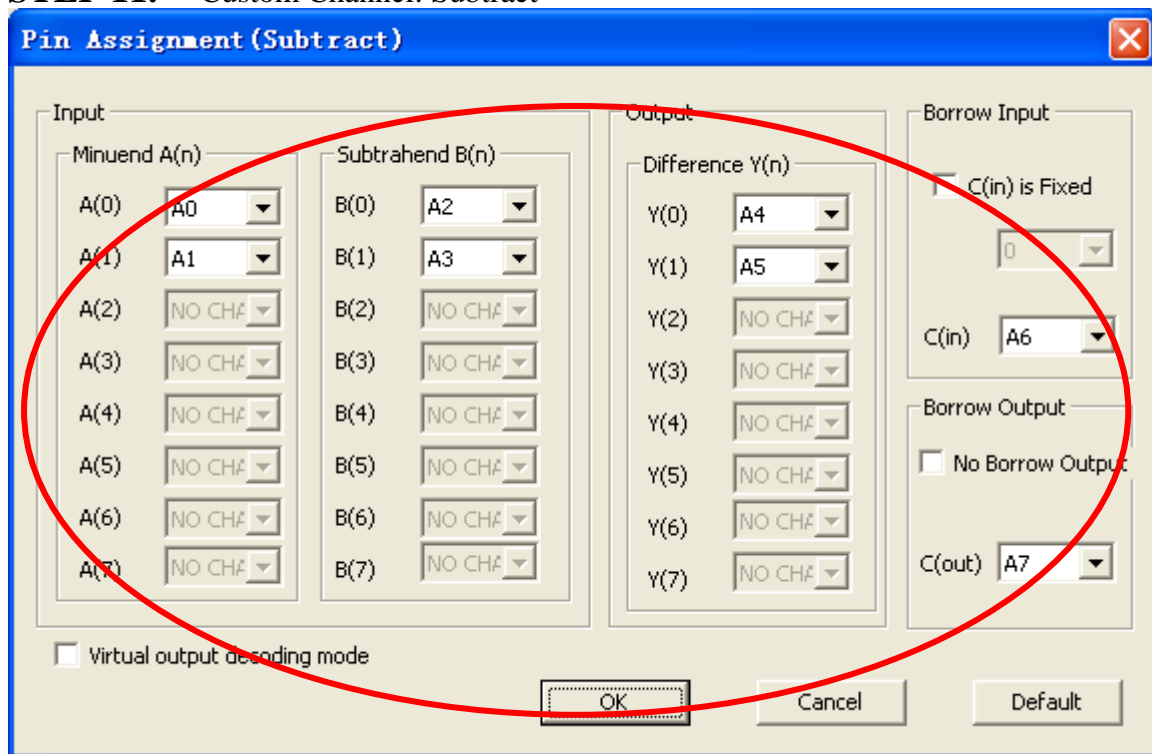
STEP 9. When user selects the different arithmetical elements, the corresponding arithmetical element channel setting will present, and user should set the required channels and the number of the channels.



STEP 10. Custom Channel: Adder



STEP 11. Custom Channel: Subtract



Pin Assignment (Subtract)

Input

Minuend A(n)	Subtrahend B(n)
A(0) A0	B(0) A2
A(1) A1	B(1) A3
A(2) NO CHA	B(2) NO CHA
A(3) NO CHA	B(3) NO CHA
A(4) NO CHA	B(4) NO CHA
A(5) NO CHA	B(5) NO CHA
A(6) NO CHA	B(6) NO CHA
A(7) NO CHA	B(7) NO CHA

Output

Difference Y(n)
Y(0) A4
Y(1) A5
Y(2) NO CHA
Y(3) NO CHA
Y(4) NO CHA
Y(5) NO CHA
Y(6) NO CHA
Y(7) NO CHA

Borrow Input

C(in) is Fixed

C(in) 0

C(in) A6

Borrow Output

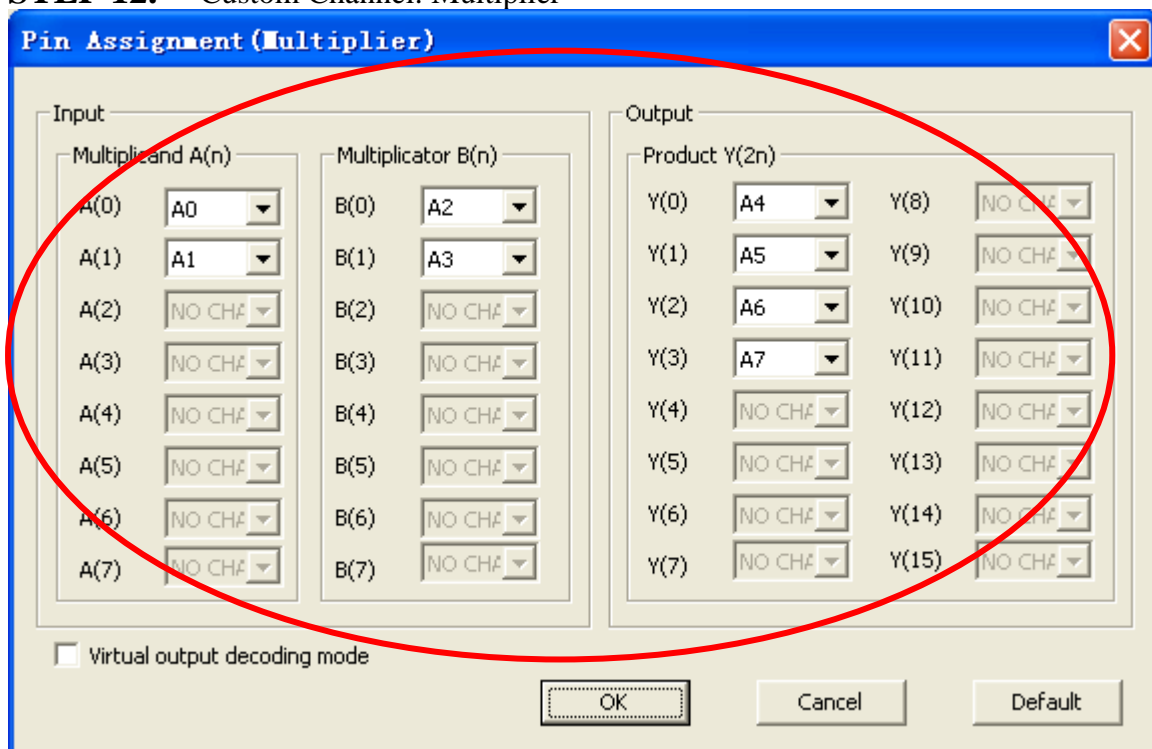
No Borrow Output

C(out) A7

Virtual output decoding mode

OK Cancel Default

STEP 12. Custom Channel: Multiplier



Pin Assignment (Multiplier)

Input

Multiplicand A(n)	Multiplicator B(n)
A(0) A0	B(0) A2
A(1) A1	B(1) A3
A(2) NO CHA	B(2) NO CHA
A(3) NO CHA	B(3) NO CHA
A(4) NO CHA	B(4) NO CHA
A(5) NO CHA	B(5) NO CHA
A(6) NO CHA	B(6) NO CHA
A(7) NO CHA	B(7) NO CHA

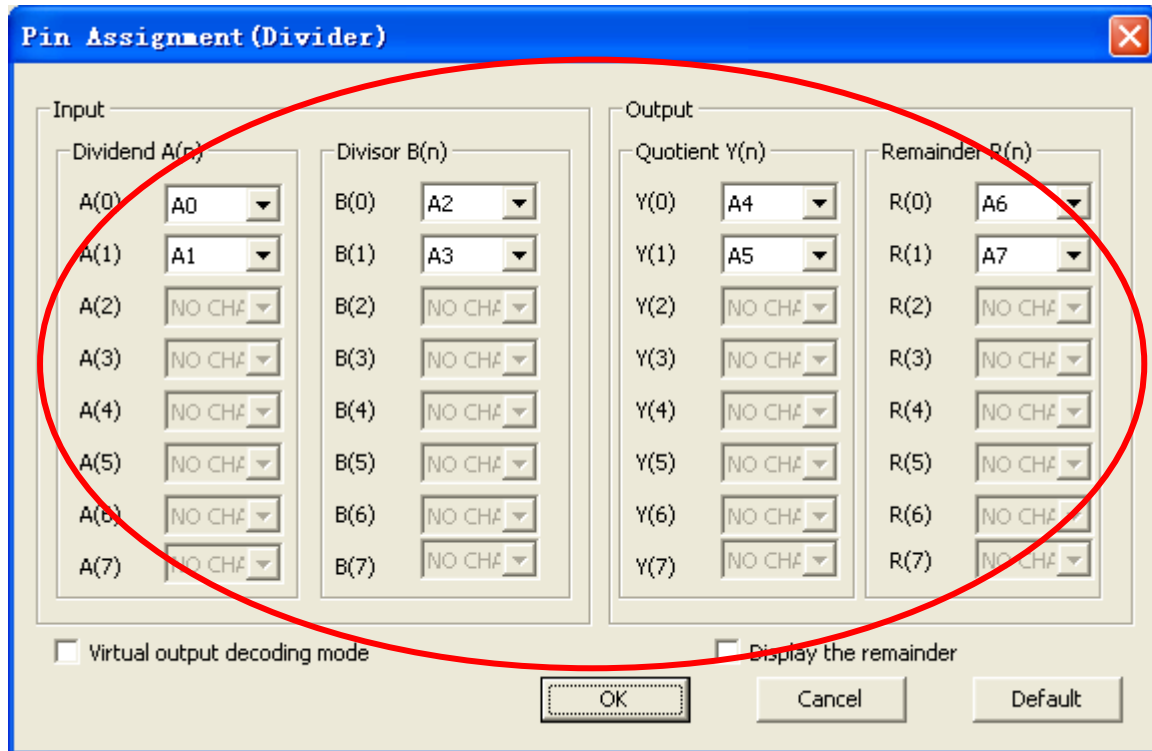
Output

Product Y(2n)	
Y(0) A4	Y(8) NO CHA
Y(1) A5	Y(9) NO CHA
Y(2) A6	Y(10) NO CHA
Y(3) A7	Y(11) NO CHA
Y(4) NO CHA	Y(12) NO CHA
Y(5) NO CHA	Y(13) NO CHA
Y(6) NO CHA	Y(14) NO CHA
Y(7) NO CHA	Y(15) NO CHA

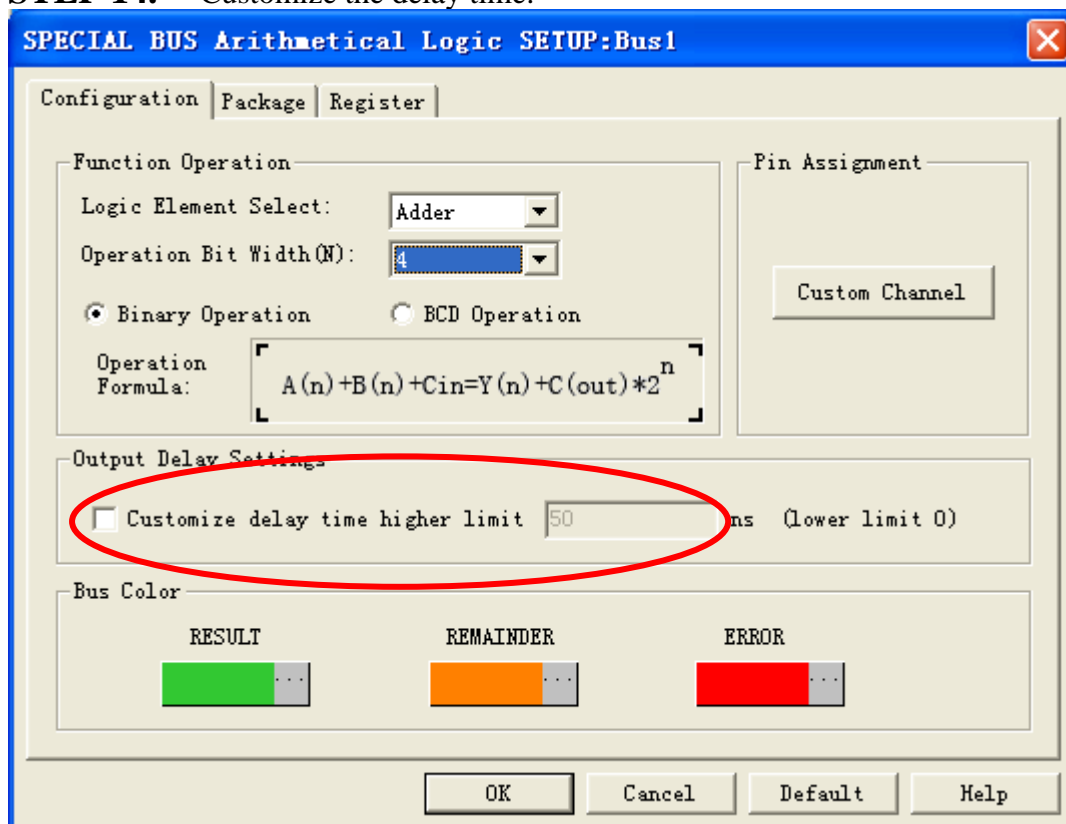
Virtual output decoding mode

OK Cancel Default

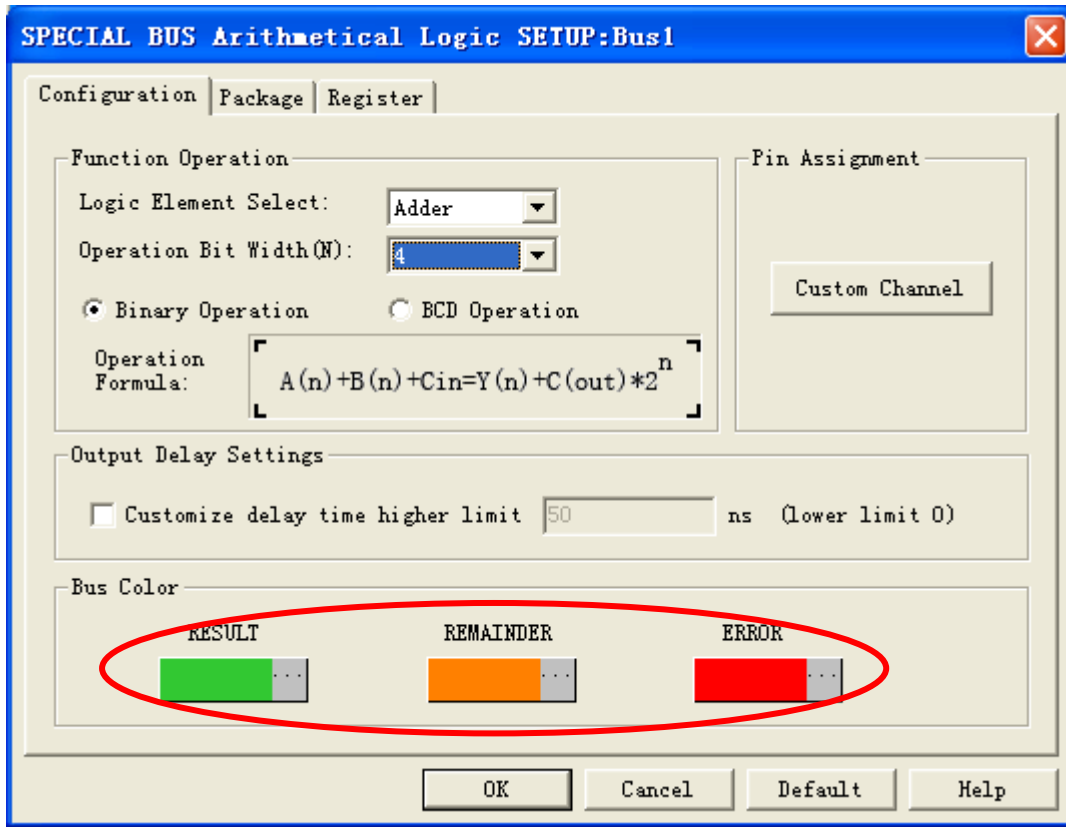
STEP 13. Custom Channel: Divider



STEP 14. Customize the delay time.

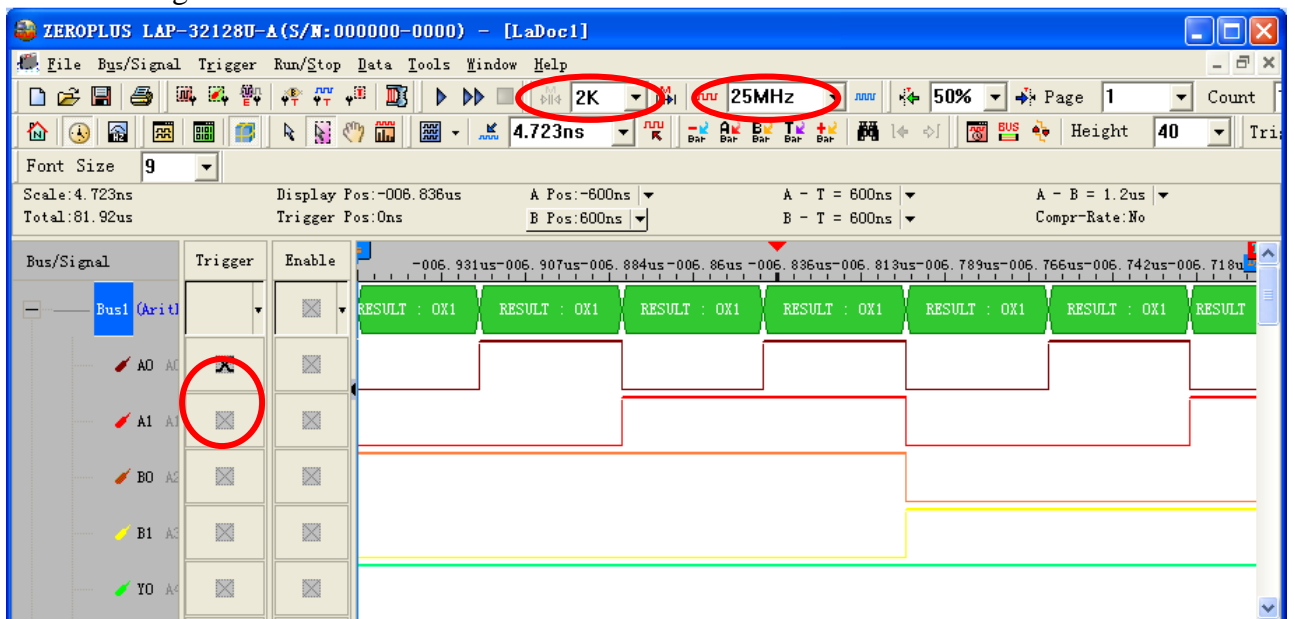


STEP 15. Set the color of the bus



STEP 16. Following pictures show the completion of the Bus decoding and package list. The conditions are set as either edge, the Memory depth is 2K, Sampling frequency is 25MHz

Bus Decoding



Package List

The screenshot shows a logic analyzer window titled "ZEROPLUS LAP-32128U-A(S/W:000000-0000) - [LaDoc1]". The interface includes a menu bar, a toolbar with various analysis tools, and a main display area. The main display shows a timing diagram with a horizontal axis representing time in microseconds (007.167u to 007.98u) and a vertical axis for signals. A red signal line shows a series of pulses, and a yellow signal line shows a single pulse. The results of the analysis are displayed in a table below the waveform.

Package #	Name	TimeStamp	RESULT
1	Bus1(Arithmetical Logic)	-040.92us	0X0
2	Bus1(Arithmetical Logic)	-040.88us	0X0
3	Bus1(Arithmetical Logic)	-040.84us	0X0
4	Bus1(Arithmetical Logic)	-040.8us	0X0