

The Zeroplus Logic Analyzer User's Manual V3.11







FM07I4A



## Index

1	Feat	ures of Zeroplus Logic Analyzer	5
	1.1	Package Contents	6
	1.2	Introduction	8
	1.3	Hardware Specifications	11
	1.4	System Requirements	14
	1.4.1	1 Operating System Requirements	14
	1.4.2	2 Hardware System Requirements	14
	1.5	Device Maintenance and Safety	15
2	Insta	allation	17
	2.1	Software Installation	18
	2.2	Hardware Installation	20
	2.3 Ti	ps and Advice	22
3	User	r Interface	23
	3.1	Menu & Tool Bars	26
	3.2	Find Data Value	76
	3.3	Statistics Feature	80
	3.4	Customize Interface	83
	3.4.1	1 Modify Waveform Display Mode	84
	3.4.2	2 Modify Ruler Mode	85
	3.4.3	3 Modify Waveform Height & Correlated Setting	86
	3.5	Auto Save	89
	3.6	Color Setting	90
	3.6.1	1 Modify Workaround Color	92
	3.6.2	2 Modify Waveform Color	93
	3.7 The	e Flow of Software Operation	94
4	Intro	duction to Logic Analysis	95
	4.1	Logic Analysis	96
	4.2	Bus Logic Analysis	108
	4.3	Plug Analysis	110
	4.4	Bus Packet List	113
	4.5	Bus Analysis	120
	4.5.1	1 Bus Analysis	121
	4.5.2	2 I2C Analysis	124
	4.5.3	3 UART Analysis	130
	4.5.4	1 SPI Analysis	135

孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

	4.5.5	5 1-WIRE Analysis	140
	4.5.6	6 HDQ Analysis	
	4.5.7	-	
	4.6	Compression	
	4.6.1	•	
	4.7	Signal Filter and Filter Delay	
	4.7.1		
	4.8	Noise Filter	
	4.8.1		
	4.9	Data Contrast	
	4.9.1		
	4.10	Refresh Protocol Analyzer	
	4.10	-	
	4.11	Memory Analyzer	
	4.11		
	4.12	Multi-stacked Logic Analyzer Settings	
	4.12		
	4.13	DSO-stacked Settings	
5	Trou	bleshooting	
	5.1	Installation Troubleshooting	
	5.2	Software Troubleshooting	
	5.3	Hardware Troubleshooting	
6	FAQ		
	6.1	Hardware	
	6.2	Software	
	6.3	Registration	
	6.4	Technical Information	
	6.5 (	Others	
7	Appe	endix	209
	7.1	Hot Keys	
	7.2	Contact Us	





This Quick Start Guide is designed to help new and intermediate users navigate and perform common tasks with the Zeroplus Logic Analyzer. Despite its simple packaging and interface, the Logic Analyzer is a sophisticated measurement and analysis tool. It is also a highly sensitive electrical current sensing device. Users must carefully read instructions and procedures pertaining to installation and operation. Any instrument connected to the unit should be properly grounded. A pair of anti-static gloves is strongly recommended when performing a task with the device. To ensure accuracy and consistency of output data, use of the bundled components is strongly recommended.

Users' opinions are very important to Zeroplus. Please contact our engineering team by telephone, fax or email with your questions or feedback. Thank you for choosing the Zeroplus Logic Analyzer.

Notice: We will not have additional notice for you, when there is any modification of the User Manual. If there is some unconformity caused by the software version upgrade, users should take the software as the standard.



# 1 Features of Zeroplus Logic Analyzer

- 1.1 Package Contents
- 1.2 Introduction
- 1.3 Hardware Specifications
- 1.4 System Requirements
- 1.5 Device Maintenance and Safety



## Objective

In this chapter, users will learn about the package contents, description, hardware specifications, system requirements, and safety issues of the Zeroplus Logic Analyzer. Although this chapter is purely informative, we highly recommend reading this carefully to ensure safety and accuracy when performing any operation with the Zeroplus Logic Analyzer.

## 1.1 Package Contents

Verify the package contents before discarding packing materials. The following components should be included in your product. For assistance, please contact our nearest distributor.

Models	LAP-	LAP-	LAP-	LAP-	LAP-	LAP-
woders	16032U	16064U	16128U	32128U-A	321000U-A	322000U-A
Logic Analyzer	1	1	1	1	1	1
16-Pin Testing Cable	0	0	0	1	1	1
8-Pin Testing Cable	2	2	2	2	2	2
Probe	2	20	20	36	36	36
USB Cable	1	1	1	1	1	1
Quick Start Guide	0	1	1	1	1	1
Driver CD**	1	1	1	1	1	1
1-Pin Testing Cable (White)	1	1	1	1	1	1
2-Pin Testing Cable (Black)	1	1	1	1	1	1

Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (162000)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)
Logic Analyzer	1	1	1	1	1	1	1
16-Pin Testing Cable	0	0	0	0	1	1	1
8-Pin Testing Cable	2	2	2	2	2	2	2
Probe	2	20	20	20	36	36	36
USB Cable	1	1	1	1	1	1	1
Quick Start Guide	0	1	1	1	1	1	1



Driver CD**	1	1	1	1	1	1	1
1-Pin Testing Cable (White)	1	1	1	1	1	1	1
2-Pin Testing Cable (Black)	1	1	1	1	1	1	1

\* This Driver CD consists of a multilingual software interface program, as well as a multilingual User Manual.

\* The following is the accessory package of LAP-C Series, the LAP-A Series is the same with LAP-C Series.



Fig. 1-1: Logic Analyzer

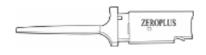


Fig. 1-3: Probe (varied depending on models)



Fig. 1-5: Quick Start Guide

Fig. 1-7: 1-Pin External Clock Cable (White)



16-Pin x 1 8-Pin x 2 Fig. 1-2: Testing Cable



Fig. 1-4: USB Cable

0

Fig. 1-6: Driver CD



Fig. 1-8: 2-Pin Ground Cable (Black)



## 1.2 Introduction

1. Zeroplus Logic Analyzer models LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A, LAP-321000U-A, and LAP-322000U-A, all share the same external features as illustrated in the following figures.

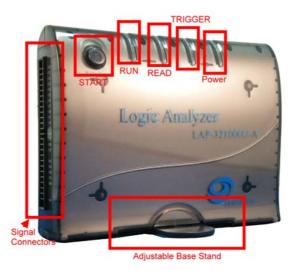


Fig. 1-9 A view of the Zeroplus Logic Analyzer LAP-A Series. See *Fig 1-12* for detailed information on the **Signal Connectors**.



Fig. 1-10 Side view of Zeroplus Logic Analyzer, which draws its power from the USB connection.

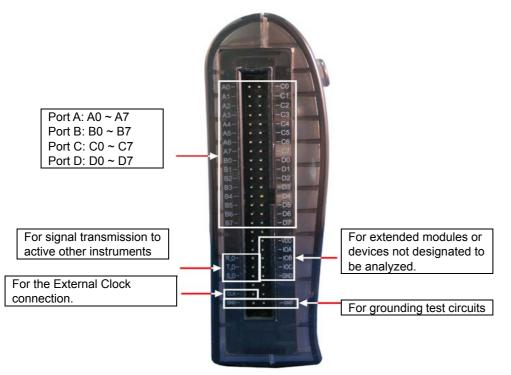


Fig. 1-11 Rear view of Zeroplus Logic Analyzer LAP-A Series



2. Zeroplus Logic Analyzer LAP-C Series share the same external features as illustrated in the following figures.



Fig. 1-12: A View of the Zeroplus Logic Analyzer LAP-C Series. See *Fig 1-11* for detailed information on the **Signal Connectors** 



Fig. 1-13: Side View of the Zeroplus Logic Analyzer; the power of the Logic Analyzer is drawn from the USB connection.

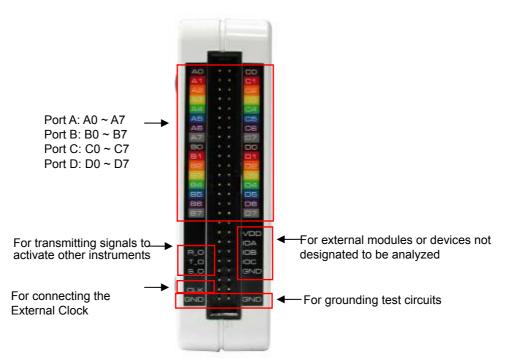


Fig. 1.14 Side View of the Zeroplus Logic Analyzer LAP-C Series



Models	LAP- 16032U	LAP- 16064U	LAP- 16128U	LAP- 32128U-A	LAP- 32100U-A	LAP- 322000U-A	
Port A ( <b>A0~A7</b> )	$\checkmark$			$\checkmark$	$\checkmark$		
Port B ( <b>B0~B7</b> )	1			$\checkmark$	$\checkmark$		
Port C ( <b>49abie7)</b> -:	X			$\checkmark$	$\checkmark$		
Port D ( <b>D0~D7</b> )	Х		$\checkmark$	$\checkmark$			
R_O		$\checkmark$		$\checkmark$	٦	1	
T_0		$\checkmark$		$\checkmark$	٦	1	
S_0	$\checkmark$		$\checkmark$	$\checkmark$			
CLK	$\checkmark$						
GND		$\checkmark$		$\checkmark$			

#### Table 1-2A: List of Functional Pins in Each Model

#### Table 1-2B: List of Functional Pins in Each Model

Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (162000)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)	
Port A ( <b>A0~A7</b> )			$\checkmark$		$\checkmark$		N	
Port B ( <b>B0~B7</b> )			$\checkmark$		$\checkmark$		N	
Port C ( <b>C0~C7</b> )			Х		$\checkmark$		V	
Port D ( <b>D0~D7</b> )		Х				$\checkmark$ $\checkmark$		
R_O			$\checkmark$		$\checkmark$		$\checkmark$	
T_O			$\checkmark$		$\checkmark$		$\checkmark$	
S_O			$\checkmark$		$\checkmark$		$\checkmark$	
CLK			$\checkmark$		$\checkmark$		$\checkmark$	
GND			$\checkmark$		$\checkmark$		$\checkmark$	
VDD	$\checkmark$			$\checkmark$		$\checkmark$		
IOA					$\checkmark$			
IOB	$\checkmark$				$\checkmark$			
IOC		$\checkmark$						
GND					$\checkmark$			

#### Table1-3: Definitions and Functions of Pins for All Models

CLK	Clock	Connect a given external module to be analyzed.
GND	Ground	Two pins used for grounding the Logic Analyzer with a given external module to be analyzed.

#### Table1-4: Definitions and Functions of Pins for Advanced Models (1)

R_O	Read (Out)	When the Logic Analyzer is about to upload data from the memory to the PC, the <b>R_O</b> will send a <b>Rising Edge</b> signal of DC3.3V. When the upload is finished, a <b>Falling Edge</b> signal is sent.
T_0	Trigger (Out)	When a trigger condition is established, the <b>T_O</b> will send a <b>Rising Edge</b> signal of DC3.3V. When the memory is full, a <b>Falling Edge</b> signal is sent.
S_0	Start (Out)	When a user initiates a sampling task by clicking the RUN



icon in the window or clicking the START button on the
device, the <b>S_O</b> will send a <b>Rising Edge</b> signal of DC3.3V.
When the Logic Analyzer finishes uploading, a Falling Edge
signal is sent.

#### Table1-5: Definitions and Functions of Pins for Advanced Models (2)

VDD	Voltage Drain (Semiconductor)	Provide +3.3 V for external modules by draining voltage from the Logic Analyzer.
ΙΟΑ	Ext. I/O Module A	Transmit signals between an external model or device and the Logic Analyzer.
IOB	Ext. I/O Module B	Same as IOA.
IOC	Ext. I/O Module C	Same as <b>IOA</b> .
GND	Ground	Ground external devices in sequence.

## **1.3 Hardware Specifications**

#### Table 1-6A: Hardware Specifications of LAP-A Series

lt a ma	) <b>T</b>	LAP-	LAP-	LAP-	LAP-	LAP-	LAP-			
Items	s\Type	16032U	16064U	16128U	32128U-A	321000U-A	322000U-A			
Inte	rface	USB 2.0 (1.1)								
Operatin	g System	Windows 2000/ Windows XP/ Windows Vista/ Windows 7								
Power	Supply			USB 1.1	(USB 2.0 Re	commended)				
Cha	nnels		16			32				
	Internal Clock Rate (asynchronous)	100Hz ~	100MHz		1(	00Hz ~ 200MHz				
Sampling Rate	Max External Clock (synchronous)	Max 7	′5MHz	Max 100MHz						
	Bandwidth				75MHz					
	Memory	512K Bits	1M Bits	4M Bits	4M Bits	32M Bits	64M Bits			
Memory	Memory Depth (Per Channel)	32K Bits 64K Bits		128K Bits	128K Bits	1M Bits	2M Bits			
	Trigger Channel	1	6 Channels	;		32 Channe	els			
	Trigger Condition									
Trigger	Pre-Trigger/ Post-Trigger	Yes								
	Trigger Level	1 Level								
	Trigger Count				1~65535					
Threshold	Working Voltage			-6V~+6V						
Voltage	Accuracy				±0.1V					



	I2C				Free						
	UART		Free								
Protocol	SPI		Free								
Analyzer	1-WIRE		Option			Free					
(Кеер	CAN 2.0B		Op	otion			Free				
Increasing)	HDQ		Op	otion			Free				
	7-SEGMEN T LED				Free						
	Operating Interface Language			Chinese	e(Si)/ Chinese	(Tr)/ English					
	Time Base Range				5ps~10Ms	;					
	Vertical Sizing		1~5.5								
	Compression	Max 8Mbits	Max 16Mbits	Max 512Mbits							
	Waveform Width Display	Yes									
	Trigger Page				1~8192Pag	е					
Software	Pulse Width Trigger				Free						
Function	Double Mode				Yes						
	Trigger Mark		Free								
	Latch Function	Option	Option	Option	Option	Free	Free				
	Data Contrast	Option	Option	Option	Option	Free	Free				
	Multi-stacked Logic Analyzer Settings	No	No	No	Yes	Yes	Yes				
	Protocol Analyzer Trigger			Optior	1		Free				
Safety Cer	rtification			FC	C/CE/WEEE/	RoHS					

#### Table 1-6B: Hardware Specifications of LAP-C Series

Items	Items\Type						LAP-C (321000)	LAP-C (322000)			
Inte	rface	USB 2.0 (1.1)									
Operating System		Windows 2000/ Windows XP/ Windows Vista/ Windows 7									
Power	Power Supply		USB 1.1 (USB 2.0 Recommended)								
Channels		16 32									
Sampling Rate	Internal Clock Rate (asynchronous)	100Hz ~	100MHz	100Hz ~ 200MHz							



Max External Clock (synchronous)         Max 75MHz         Max 100MHz           Bendwidth         75MHz         Max 100MHz           Memory Depth (Per Channel)         512K Bits         1M Bits         4M Bits         64M Bits         4M Bits         32M Bits         64M Bits           Trigger Channel         32K Bits         64K Bits         128K Bits         11M Bits         2M Bits												
Memory Depti512K Bits1M Bits4M Bits64M Bits4M Bits32M Bits64M BitsMemory Depti32K Bits64K Bits128K Bits128K Bits11 Bits2M Bits2M Bits11 Bits2M Bits2M BitsTrigger Condition32K Bits64K Bits128K Bits128K Bits11 Bits2M Bits2M Bits11 Bits2M BitsTrigger ConditionTrigger Pre-Trigger/ Pre-Trigger/ Pre-Trigger/ Pre-Trigger/ Pre-Trigger/ Trigger Level16 Channell128K Bits11 M Bits2M Bits2M BitsTrigger Pre-Trigger/ Post-Trigger Pre-Trigger/ Post-Trigger16 Channell16 Channell128K Bits14 M Bits2M Bits2M BitsTrigger Post-Trigger VoltageAccuracy1< Level1< Level111		External Clock	Max 7	′5MHz			Max 100MH	Z				
Memory         Memory         Memory         Depth (Per Caname)         32K Bits         64K Bits         128K Bits         1M Bits         2M Bits         1M Bits         2M Bits         1M Bits         2M Bits         2M Bits         2M Bits         1M Bits         2M Bits         2M Bits         1M Bits         2M Bits         2M Bits         1M Bits         2M Bits <th></th> <th>Bandwidth</th> <th></th> <th></th> <th></th> <th></th> <th></th>		Bandwidth										
Memory Deph (Pr Deph (Pr Channel)32K Bits64K Bits128K Bits2M Bits1128K Bits11M Bits2M BitsTrigger 		Memory	512K Bits	1M Bits	4M Bits	64M Bits	4M Bits	32M Bits	64M Bits			
TriggerVersion leftYesTringerYesFreeTringerYesTringerYesTringerYesTringerYesTringerYesTringerYesTringerYesTringer leftTringerYesYesTringerYesTringerYesTringerYesTringerYesTringer <t< th=""><th>Memory</th><td>Depth (Per</td><td>32K Bits</td><td>64K Bits</td><td>128K Bits</td><td>2M Bits</td><td>128K Bits</td><td>1M Bits</td><td>2M Bits</td></t<>	Memory	Depth (Per	32K Bits	64K Bits	128K Bits	2M Bits	128K Bits	1M Bits	2M Bits			
Trigger Condition         Pattern/Edge           Trigger Prot-Trigger Post-Trigger Contraition         Yes           Trigger Level         Yes           Trigger Count         1 Level           Trigger Count         Yes           Trigger Count         1 Level           Trigger Count         Jestimation of the state				16 Cł	nannels			32 Channels	;			
Trigger Post-Trigger/ Post-Trigger LevelYesTrigger Level1 LevelTrigger Count1 -65535Threshold VoltageWorking Voltage $-6V - 46V$ Voltage $1 - 2000$ Accuracy $\pm 0.1V$ I2C $Free$ UART $Free$ UART $Free$ INPRE $Option$ 1.WIRE $Option$ Free $Option$ Software $Max$ MaxMax Compression $Max$ Max Max Max Max Max Max 		Trigger				Pattern/Edg	ge					
Trigger Count1~65535Threshold VoltageWorking Voltage-6V~+6VVoltage-6V~+6VAccuracy±0.1VI2CFreeUARTFreeUARTFreeMalyzerI2CAnalyzerFreeIncreasing)HDQOptionFreeIncreasing)HDQOptionFreeOperating Interface LanguageIncreasingMax Vartical SizingMax Max	Trigger	Pre-Trigger/				Yes						
Morking Voltage       -6V~+6V         Working Voltage       -6V~+6V         Accuracy $\pm 0.1V$ I2C $\pm 0.1V$ UART       Free         UART       Free         Option       Free         Analyzer       CAN 2.0B       Option       Free         Increasing)       HDQ       Option       Free       Option       Free         More fill       Option       Free       Option       Free         Mone fill       Option       Free       Option       Free         Increasing)       HDQ       Option       Free       Secondary         Mox       Max       Max       Max       Max       Max       Max         Vertical Sizing       Max       <		Trigger Level				1 Level						
Morking Voltage         Working Voltage         -6V-+6V           Accuracy $\pm 0.1V$ I2C         Free           UART         Free           Voltage         SPI           12C         Free           Manalyzer         1-WIRE           IAWRE         Option           Free         Option           Manalyzer         1-WIRE           MDQ         Option           Free         Option           Free         Option           T-ED         Free           Operating Interface         Chinese(Si)/ Chinese(Tr)/ English           Interface         Chinese(Si)/ Chinese(Tr)/ English           Interface         String           Vertical         32Mbits           String         1-~5.5           String         16Mbits           Vertical         32Mbits           String         16Mbits           Trigger Page         1-~8192Page           Free         Pulse Width           Trigger Page         1-~8192Page           Trigger Mark         Option           Free         Option           Double Mode         No           Data		Trigger Count				1~65535						
VoltageAccuracy $\pm \cdot \cdot$	Threshold	Working				-6V~+6V						
ProtocolSPIFreeAnalyzer1-WIREOptionFreeOptionFree1-WIREOptionFreeOptionFree(KeepCAN 2.0BOptionFreeOptionFreeIncreasing)HDQOptionFreeFree7-SEGMEN T LEDTEDFreeFreeOperating Interface LanguageOptionFreeVertical SizingOptionFreeVertical DisplayMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsMax 32MbitsYesFreePulse Width Trigger PageFreeOptionFreePulse Width DisplayTrigger AgeYesTrigger Mark Data ContrastOptionFreeOptionFreeData ContrastOptionFreeOptionFreeMulti-stackedNoYesYes	Voltage					±0.1V						
ProtocolSPIFreeAnalyzer1-WIREOptionFreeOptionFree(KeepCAN 2.0BOptionFreeOptionFreeIncreasing)HDQOptionFreeSectionFree7-SEGMEN T LEDTegOptionFreeFreeOperating Interface LanguageOperating Interface LanguageChinese(Si)/ Chinese(Tr/) EnglishTime Base RangeSps-10MsMaxMaxMax MaxMax StizingStizingMax StizingMax StizingMax StizingStiz		I2C				Free						
Analyzer (Keep1-WIREOptionFree $Free$ Option $Free$ (Keep Increasing)HDQ $\bigcirc$ Option $Free$ $Option$ $Free$ 7-SEGMEN T LED $TLED$ $Free$ $Free$ $Free$ Operating Interface $OperatingInterfaceChinese(Si)/ Chinese(Tr)/ EnglishFreeTime BaseTrime Base1\sim 5, 5SizingSizingVerticalSizingSizing1\sim 5, 5SizingMax16MbitsMax32MbitsMax512MbitsMaxStabitsMax$		UART		Free								
$\begin{tabular}{ c c c c c } \hline CAN 2.0B & Option & Free & Option & Free \\ \hline Increasing) & HDQ & Option & Free \\ \hline TABLE & Free & Free & Free \\ \hline TABLE & Chinese(Si)/ Chinese(Tr)/ English & Language \\ \hline Time Base & Sps~10Ms & Sps~10Ms & Max & Ma$	Protocol	SPI	Free									
Increasing)HDQOptionFree7-SEGMENTLEDFreeFreeT LEDChinese(Si)/ Chinese(Tr)/ EnglishInterface LanguageChinese(Si)/ Chinese(Tr)/ EnglishTime BaseSps~10MsRangeSizingVertical Sizing1~5.5CompressionMax 8MbitsMax 16MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsSoftwareWaveform Width DisplayMax SizingMax 16MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsFunctionMax DisplayMax SoftwareMax SizingMax SizingMax SizingMax SizingMax SizingMax SizingFreeMut DisplaySizingSizingSizingSizingSizingTrigger PageImageImageYesSizingSizingTrigger PageImageImageFreeFreeDouble ModeNoYesFreeLatch FunctionOptionFreeOptionFreeData ContrastOptionFreeOptionFreeMuti-stackedNoYesYes	Analyzer	1-WIRE		Option			Fre	ee				
7-SEGMEN T LEDFreeOperating Interface LanguageChinese(Si)/ Chinese(Tr)/ EnglishTime Base Range Vertical Sizing $1\sim5.5$ CompressionMax 8MbitsMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsMax 255MbitsMax 512MbitsSoftware FunctionWaveform Width DisplayMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsMax 255MbitsMax 512MbitsTrigger PageTrigger PageT-8192PageVersTrigger MarkOptionFreePreeDouble ModeNoYesTrigger MarkOptionFreeData ContrastOptionFreeMutti-stackedNoFreeOptionFreeMutti-stackedNoFreeOptionFree	(Keep	CAN 2.0B		Option		Free	Option	Fre	e			
FreeOperating Interface LanguageTime Base Range Vertical Sizing $5ps \sim 10Ms$ Vertical Sizing $1 \sim 5.5$ CompressionMax 8MbitsMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsVaveform Width DisplayMax Trigger PageMax Trigger MarkMax OptionMax FreeMax SoftwareFunctionNoVersVersVersVersVersIntegerSoftwareSoftwareFreeOptionFreeIntegerSoftwareSoftwareFreeOptionFreeIntegerSoftwareSoftwareFreeOptionFreeIntegerSoftwareSoftwareFre	Increasing)	HDQ			Option	Option			ee			
Interface LanguageChinese(Si)/ Chinese(Tr)/ EnglishTime Base RangeTime Base RangeVertical Sizing $1\sim5.5$ CompressionMax 8MbitsMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsMax 255MbitsMax 512MbitsSoftware FunctionWaveform Width DisplayMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsMax 255MbitsMax 512MbitsPulse Width Trigger PageTrigger PageTreeTreePulse Width Trigger MarkOptionFreeOptionFreeDouble ModeNoYesFreeDouble ModeOptionFreeOptionFreeLatch Data ContrastOptionFreeOptionFreeMutti-stackedNoYesYes			Free									
Time Base RangeSps~10MsVertical Sizing $1\sim5.5$ CompressionMax 8MbitsMax 16MbitsMax 32MbitsMax 512MbitsMax 32MbitsMax 255MbitsMax 512MbitsFunctionWaveform Width DisplayVertical 16MbitsYesVertical 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsMax 32MbitsFunctionWaveform Width DisplayVertical 16MbitsYesVertical 32MbitsMax 32Mbits <t< th=""><th></th><th>Interface</th><th></th><th></th><th>Chinese</th><th>(Si)/ Chinese</th><th>e(Tr)/ English</th><th>I</th><th></th></t<>		Interface			Chinese	(Si)/ Chinese	e(Tr)/ English	I				
Vertical SizingVertical Sizing1~5.5CompressionMax 8MbitsMax 16MbitsMax 32MbitsMax 512MbitsMax 255MbitsMax 512MbitsFunctionWaveform Width DisplayWaveform Width DisplayYesVertical 255MbitsS12MbitsTrigger Page		Time Base				5ps~10Ms	3					
Software     Max 8Mbits     Max 16Mbits     Max 32Mbits     Max 512Mbits     Max 32Mbits     Max 32M		Vertical				1~5.5						
Width Display       Yes         Trigger Page       1~8192Page         Pulse Width Trigger       Free         Double Mode       No         Yes         Double Mode       No         Trigger Mark       Option         Free       Option         Latch Function       Option         Data Contrast       Option         Multi-stacked       No         Yes												
Display       Inclusion		Width				Yes						
Pulse Width Trigger     Free       Double Mode     No       Trigger Mark     Option       Free     Option       Free     Option       Free     Option       Latch Function     Option       Data Contrast     Option       Multi-stacked     No						1~8192Par	1e					
Trigger     No     Yes       Double Mode     No     Yes       Trigger Mark     Option     Free     Option     Free       Latch     Option     Free     Option     Free       Data     Option     Free     Option     Free       Data     Option     Free     Option     Free       Multi-stacked     No     Yes												
Trigger Mark     Option     Free     Option     Free       Latch     Option     Free     Option     Free       Data     Option     Free     Option     Free       Data     Option     Free     Option     Free       Multi-stacked     No     Yes						Free	Free					
Latch     Option     Free     Option     Free       Data     Option     Free     Option     Free       Contrast     Option     Free     Option     Free			N	0			Yes					
Function     Option     Free     Option     Free       Data     Option     Free     Option     Free       Contrast     Option     Free     Ves		Trigger Mark		Option		Free	Opt	ion	Free			
Contrast     Option     Free     Option     Free       Multi-stacked     No     Yes				Option		Free	Option	Fre	e			
				Option		Free	Option	Fre	ee			
				1	No			Yes				

Logic



Analyzer Settings		
Protocol Analyzer Trigger	Option	Free
Safety Certification	FCC/CE/WEEE/RoHS	

## 1.4 System Requirements

This section discusses basic operating system and hardware requirements for the Logic Analyzer. Software and hardware capabilities may vary depending on PC configuration. This manual assumes proper installation of a supported operating system as listed below.

### 1.4.1 Operating System Requirements

	Support	Non-support
Operating System Name	<ul> <li>Windows 2000</li> <li>(Professional, Server Family)</li> <li>Windows XP</li> <li>(Home, Professional Editions 32-Bit version)</li> <li>Windows VISTA</li> <li>(32-Bit and 64-Bit version)</li> <li>Windows 7</li> <li>(32-Bit and 64-Bit version)</li> </ul>	<ul> <li>Windows NT 4.0 (Workstation &amp; Server, Service Pack 6)</li> <li>Windows Server 2003</li> </ul>

### 1.4.2 Hardware System Requirements

Hardware Name	Lowest Configuration	Recommended Configuration				
CPU	166 MHz	900 MHz				
Memory	64MB	256MB				
Display Device	VGA Display Capability with 1024x768 resolution or higher.	VGA Display Capability with 1024x768 resolution or higher.				
Hard Drive	At least 100MB available space	At least 100MB available space				
USB	USB1.1 supported	USB2.0 recommended				



## 1.5 Device Maintenance and Safety

Follow these instructions for proper operation and storage of the Logic Analyzer.

#### Table1-7: General Advice

Cautions	<ul> <li>Do not place heavy objects on the Zeroplus Logic Analyzer.</li> <li>Avoid hard impacts and rough handling.</li> <li>Protect the Logic Analyzer from static discharge.</li> <li>Do not disassemble the Zeroplus Logic Analyzer; this will void the warranty and could affect its operation.</li> </ul>
Cleaning	<ul> <li>Use a soft, damp cloth with a mild detergent to clean.</li> <li>Do not spray any liquid on the Zeroplus Logic Analyzer or immerse it in any liquid.</li> <li>Do not use harsh chemicals or cleaners containing substances such as benzene, toluene, xylene or acetone.</li> </ul>

#### Table1-8: Electrical Specifications(LAP-A Series & LAP-C Series)

Items	Minimum	Typical	Maximum
Working Voltage	DC 4.5 V	DC 5.0 V	DC 5.5 V
Current at Rest			200 mA
Current at Work			400 mA
Power at Rest			1 W
Power at Work			2W
Error in Phase Off*			1.5 nS
Vinput of Testing Channel	DC -30V		DC 30 V
V <sub>Reference</sub>	DC -6V		DC 6 V
Input Resistance		500KΩ/10pF	
Working Temperature	5°C		70°C
Storage Temperature	-40°C		80°C

\* Refer to the User Manual for error analysis calculation.



	Table1-9: Operating Environment
WARNING	<ul> <li>Avoid direct sunlight</li> <li>Use in a dust free, non-conductive environment (see Note)</li> <li>Relative Humidity: &lt; 80%</li> <li>Altitude: &lt; 2000m</li> <li>Temperature: 0 ~ 40 Degrees C</li> </ul> This is a Class A product which may cause radio interference in a domestic environment.
	Note: EN 61010-1:2001 specify degrees of pollution and their requirements. Logic Analyzer falls under Level 2.
	Pollution refers to 'addition of foreign matter, solid, liquid or gaseous (ionized gases), which may produce a reduction of dielectric strength or surface resistivity'.
	Pollution Degree 1: No pollution or only dry, non-conductive pollution occurs. This pollution has no effect.
	Pollution Degree 2: Normally only non-conductive pollution occurs. Occasionally, however, temporary conductivity caused by the condensation must be expected.
	Pollution Degree 3: Conductive pollution occurs or dry, non-conductive pollution which becomes conductive due to the condensation occurs. In such conditions, the equipment is normally protected against exposure to direct sunlight, precipitation and wind, but neither temperature nor humidity is controlled.
Storage Environment	Relative Humidity: < 80% Temperature: 0 ~ 50 Degrees C

## Conclusion

After reading this section, users should have a basic grasp of the Logic Analyzer. A complete understanding of the section, **Device Maintenance and Safety**, is a critical prerequisite of any further operation as presented in the User Manual.



# **2** Installation

- 2.1 Software Installation
- 2.2 Hardware Installation
- 2.3 Tips and Advice



## Objective

This chapter describes the installation of the Logic Analyzer hardware and software. Software installation steps must be followed precisely to ensure successful installation.

## 2.1 Software Installation

In this section, users will learn how to install the software interface and drivers. As with proper installation of many USB devices, the Logic Analyzer application and driver software must be installed prior to the connection of the hardware. The following steps illustrate an installation of a Zeroplus **LAP-C V3.11** Logic Analyzer. The other twelve models mentioned in Chapter 1 would follow identical procedures.

- Step 1. Insert the driver CD-ROM in the PC CD drive.
- Step 2. Execute the installation program. Go to the START menu, click START, Run, Browse in sequence, select Setup.exe file in the appropriate model folder and then click OK. It is recommended that all other programs are closed while the installation proceeds.
- Step 3. Choose the Application Setup.
- Step 4. Click Next to proceed with the Install Wizard.
- Step 5. Select "I accept the terms of the license agreement", and click Next.
- Step 6. Enter User and Company names.
- Step 7. Choose the setup type. We recommend Complete for most users.
- Step 8. Click Install to confirm settings and begin the actual installation.
- Step 9. Click Finish to complete the installation.





## 2.2 Hardware Installation

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

Hardware installation simply involves in connecting the Logic Analyzer to your computer with the included USB Cable as shown in Figures 2-4 and 2-5.

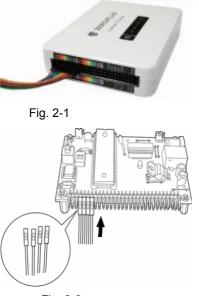


Fig. 2-2

1. Plug the fixed end of the cables into the LA (Fig. 2-1).

2. Plug the loose ends into the connectors on the circuit board to be analyzed (Fig. 2-2).

**Note:** The following sequence must be observed when connecting the connectors into the circuit board: A0 = Brown, A1 = Red, A2 = Orange, A3 = Yellow, A4 = Green, A5 = Blue, A6 = Purple and A7 = Gray.

3. The circuit board must be grounded to the Logic Analyzer with the black Ground Cable (Fig. 2-3).



Fig. 2-3

Fig. 2-4



Fig. 2-5

5. Plug the thin end into the computer (Fig. 2-5).

4. Plug the square end of the USB cable into the Logic Analyzer (Fig. 2-4).



At this point, the computer should be able to detect the Logic Analyzer and finalize the installation for hardware connection. For further information, refer to the Troubleshooting and Frequently Asked Questions (FAQ) chapters in the User Manual.



Fig. 2-6: An Assembly of Laptop, Logic Analyzer and Testing Board of LAP-C Series

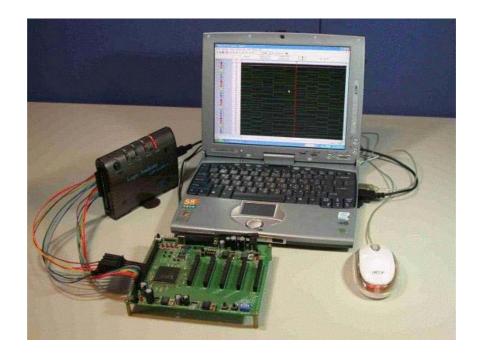
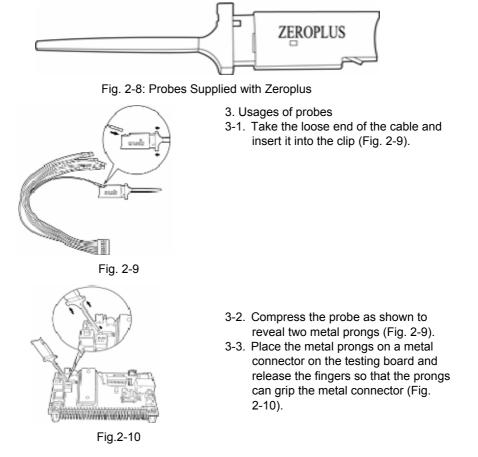


Fig.2-7 An Assembly of Laptop, Logic Analyzer and Testing Board of LAP-A Series



## 2.3 Tips and Advice

- 1. When testing a circuit board, make sure that the internal sampling frequency (within the Logic Analyzer) is at least four times higher than the external board frequency.
- 2. If the signal connector does not work well with the pins on the test board, try to use the supplied probes.



- 4. The Logic Analyzer will connect to the **Zeroplus** server for software updates if an internet connection is available.
- 5. Unwanted signals can be filtered out using the Signal Filter or Filter Delay functions.
- 6. When measuring for a long period, **Compression** makes memory more efficient.
- 7. Trigger condition depends on the testing board. If triggering does not work well, try to narrow the trigger conditions and optimize them repeatedly.
- 8. If a testing board has a lower frequency than Logic Analyzer, sample signals according to the external clock.
- 9. When sampling from an external clock, filter extra signals with the Signal Filter function.
- 10. Unused channels may be removed from the Bus/Signal display using Bus/Signal (Menu) → Channels Setup.



## **3 User Interface**

- 3.1 Menu & Tool Bars
- 3.2 Find Data Value
- 3.3 Statistics Feature
- 3.4 Customize Interface
- 3.5 Auto Save
- 3.6 Color Setting
- 3.7 The Flow of Software Operation



## Objective

Chapter 3 presents detailed information on the Logic Analyzer software interface in four sections: **Menu Bar**, **Tool Bar**, **Statistical Function**, and **Interface Customization**.

## **Basic Layout**

The layout of the Logic Analyzer software interface can be divided into nine sections as shown in the following figure.

		¥T ¥		- <u>*</u>		_		_		50% -		30	-    Ti	▲ Count rigger Delar	·
le:10us al:20.48ms		Dioplay Display	Range:-2	 50us ~ 2	80us	A Pos: 14 B Pos:15	50uo <b>-</b> i0us <del>-</del>			A T = 150 B - T = 150	us 🔻			A D = 300 Compr-Rate	e:No
Bus/Signal	Trigger	Filter	$\sim$	200.00		N Duo	4	Due -	ļ	5	240	100ue	- <mark>1</mark>	0un - 20	25
🝼 AO AO		• 🖾	$\mathbf{N}$					20					$\Box$		
🝼 A1 A1			20	20 20	20 2	0 20 20	20 20 2	20 :	20 2	0 20 20	20 20	20 20	20	20 20 2	0 20 20
🥑 A2 A2			40us	40us	40u:	a 40us	40us 3	30us	40u	40us	40us	40us	40	us 40u:	s 40us
🥑 A3 A3			80	us		30us	70us			30us	80	)us		80us	80
🥑 A4 A4			160	Dus		150	)us			16	Dus			1	60us
🥑 A5 A5					3	10us						32	0us		
🥑 A6 A6					6	30us							6	40us	
<b>*5</b> <sup>A7</sup>	6	7			1	.27ms		8					1	28ms	
<b>60</b> B0										20.4	8ms				
										20.4	8ms				
🥑 <b>B2</b> B2										20.4	8ms				
🥑 B3 B3										20.4	8ms				
✓ B4 B4										20.4	8ms		_		
✓ B5 B5										20.4	8ms		_		
<b>✓ B6</b> B6										20.4	8ms				
										20.4	8ms				
<b>✓ CO</b> CO			$\wedge$							20.4	8ms				
🥑 C1 C1	$\square$									20.4	8ms				/

Fig 3-1: Software Interface

#### 1. Menu Bar

All operations are performed directly from the menu bar, including **configure label**, **rename**, **execute** and **stop**. Pull-down menus allow easy navigation through the measurement panel.

#### 2. Tool Bar

The tool bar is the graphical user interface which can make you work with some of the more common applications. From these icons, you can change settings and operate the Logic Analyzer easily.

Note: The prompting information of the shortcut keys has been added in the tooltips of the Tool Bar, that is to say, when users place the cursor on the icons, the corresponding shortcut key information will appear. For example, the prompting information of the New button is "New (Ctrl+N)". "Ctrl+N" is the Shortcut Key of the function of New.

#### 3. Information Bar

The Information Bar displays information about the grids in the waveform, such as: Address, Time, Frequency, Trigger Bar, A Bar, B Bar and other Bar. Details of the labels are below:

Scale - Define the acquisition clock that controls the data sampling

Total - The period of time when Logic Analyzer captures data.

Display Pos - The middle tip means the middle position of the waveform.

Display Range-Display the waveform time range of the current waveform display area.

- A Pos The main function is to set A Bar or the other Bar.
- B Pos The main function is to set B Bar or the other Bar.
- A-B Press the under arrow to exchange and become the other Bar

Moreover, you also can execute this function from the other Bar.

#### 4. Ruler (Waveform Display / Listing Display)

Ruler shows the time position of the waveform shown in the waveform display area or the listing display area.



#### 5. Bus/Signal (Waveform Display / Listing Display)

Edit names of the measured channels; color shown matches the trace color.

#### 6. Trigger Column

Trigger Column allows users to adjust signal trigger conditions.

### 7. Filter Column

Filter Column allows users to set Bus or signal filter conditions.

#### 8. Display Area

Acquired data is displayed as a waveform or in a list format.

#### Waveform Display

This interface shows the digital signals. When the signal is logic "0", the waveform will be displayed as \_\_\_\_\_. If the signal is logic "1", the waveform is as \_\_\_\_\_. An unknown signal waveform is displayed in gray between the high and low levels as \_\_\_\_\_. There are sixteen channels in LAP-16032U, LAP-16064U, LAP-16128U, LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(162000), and thirty two channels in LAP-32128U-A, LAP-321000U-A, LAP-322000U-A, LAP-C(32128), LAP-C(321000) and LAP-C(322000).

#### **Listing Display**

This interface shows the digital signals as 1 and 0. Logic 1 is displayed as "1" and logic 0 is displayed as "0".

#### 9. Status Area

Display Logic Analyzer status. The function name is also indicated here.



## 3.1 Menu & Tool Bars

Section 3.1 presents detailed information on the eight menu and thirteen tool items shown in the menu bar. The eight menu items are File, Bus/Signal, Trigger, Run/Stop, Data, Tools, Window and Help. The thirteen tool items are Standard, Trigger, Run/Stop, Sampling, Trigger Content Set, Display Mode, Windows, Mouse Pattern, Zoom, Data, Show Time/Height, Trigger Delay and Font Size.

## 1. File

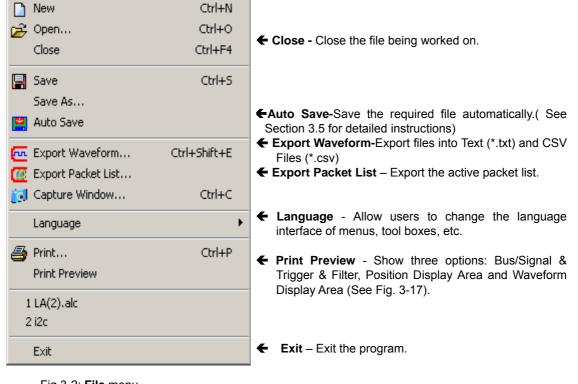


Fig 3-2: File menu.



Fig 3-3: Standard Tool Bar.

#### Menu Bar: File

Menu Ite	em	Detail Menu & Dialog Box
New	Ctrl+N	Open a <b>New</b> file.



Ctrl+O

Ctrl+F4

🔁 Open...

Close

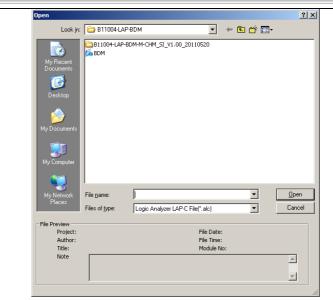


Fig 3-4: Open an existing file.

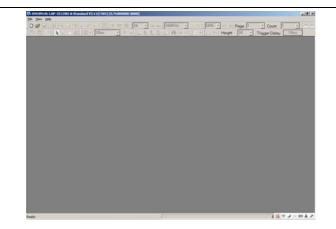
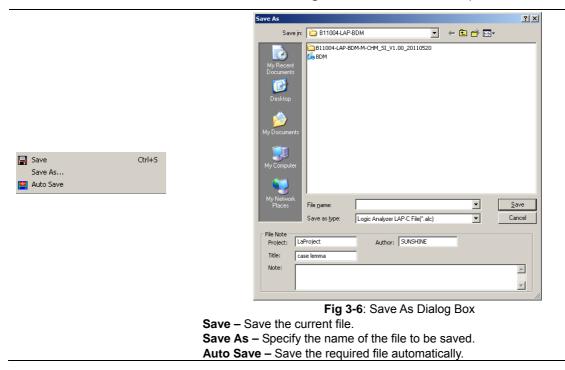


Fig 3-5: Close the active workspace.



Export Waveform	<u>? ×</u>
Savejn: 🔁 B11004-LAP-BDM 💌	← 🗈 💣 Ⅲ-
My Recert Documents Wy Documents Wy Computer	
My Network Places Save as type: Text Files(".txt)	▼ <u>S</u> ave ▼ Cancel
Bus Output Parameter - Data Information - Data Style ALL	Bus Item
Perform Model     Data Model All Data     Vertical     C Horizontal     Data Format Hexadecimal	• •
Output Range	
From A Bar To	User Defined  I0.25ms
Pop up an export file automatically	

Fig 3-7: Export Waveform Dialog Box

**Export Waveform:** Export a file into text (\*.txt) or CSV (\*.csv) formats. **Bus Output Parameter:** Decide whether or not to display the parameters of the file to be exported.

**Perform Model:** Choose whether to export the data either vertical or horizontal.

**Data Style:** Include ALL, ALL BUS, PROTOCOL (HAS CHANNELS ), PROTOCOL(NO CHANNELS).

**Data Model:** Export data changed function; the selected items inc lude ALL Data, Sampling Changed Dot (Compression), Data Cha nged Dot (Compression). Some of the data value for the signal c hannels of sampling position are the same, for example, view the data changed and decrease export capacity; this function will be good for users.

**Output Range:** Choose the range of the data to export from the pull-down menus.

**Pop up an export file automatically:** The export file can be popped up automatically. Users can decide whether to activate the function; the default is selected. See the export file below:

11.		30-1	1 + 10 - 10 + 10	- 10 - 10 - 10 - 1		(0,-1) = (0,-1) =		1 - 10					1
9		Th	anks for u	sing ZERO	PLUS Logi	Analyzer							
1				Versi	on:V3.11								
1		36 - 5	i = ii > ii > ii	- 10 - 10 - 10 - 1		M = M + M + M	M + M + M +	H - H					
	name: 11.txt size:93 kB												
	created on:												
	ic Analyzer s												
	npling mode												
	ernal samplir d size = 2kB	ig freque	ency = 10	0000 Hz									
	ie Use Data i		den .										
	e use Data		sion.										
	number of		- 33										
	oper Propert			- SON:									
; ····				t = 1.50	LIB Por	t = 1.50 V	LIC Po	d = 1.50 V	UD Po	r = 1 501	2		
1		ger cour		n - 1.30 i	1010		110.10	11 - 1.501	110.10				
1		ger bage											
	nal Filter set			on lengthe	ns or shor	tens: no							
1		ime: Dis.											
117	"stands for	the sign	al of high	pattern, 1	"L\" prese	nts the sig	nal of low	pattern an	d \"X\" m	eans don'	t care.		
/ Sig	nal Trigger s	etup : \"	D\" stands	s for don't	care, \"H\	presents	high patt	ern and \"L	" means	low patter	m.		
1.	/*	R\" mear	is Rising I	Edge, \"F\"	presents	Falling Edg	1. \"E\" \$	tands for Ei	ther.				
	display and				ing the ch	aracter of	the origin	al file to pr	esent.				
	display of n				Scale:								
eepi	ng the settin	gs is ess	ential to r	eproduce	channels	and Buses,							
	innel name	AO	AI	A2	A3	A4	AS	A6	A7	BO	81	82	
3	B4	85	86	87	CO	CI	C2	C3	C4	C5	C6	C7	
xo xo	D1	02	D3	D4	DS	06	D7	L.3	1.4	0	r.0	C/	
~~ ·	524	ME.	./3	- C.	- 20								

🚾 Export Waveform... Ctrl+Shift+E



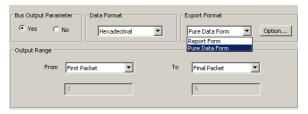
Export Packet List						<u>? ×</u>
Save in:	🚞 signal		•	+ 🗈 💣		
My Recent Documents						
Desktop						
My Documents						
My Computer						
Places	File <u>n</u> ame: Save as <u>t</u> ype:	Text Files(".txt)		•		ncel
Bus Output Paran		Format exadecimal		Format	Option	ì
Output Range						
From	First Packet	•	To Fina	al Packet	•	
	1		5			
Pop up an expo	rt file automatical	ly				//.

Fig 3-9: Export Packet List Dialog Box

Users can use paperwork, register and analyze packet list data.

**Pop up an export file automatically**: The function of popping up an export file automatically in the Export Packet List dialog box is the same with that of the Export Waveform dialog box.

**Export Format**: The Export Format is convenient for users to use the captured data in the following process. There are two formats for selecting, Report Form and Pure Data Form. See the following picture:



#### Fig 3-10: Export Format Pull-down Menu

In the part of the Export Format, when the users select the Report Form, the "Option" button can't be used; when users select the Pure Data Form, the "Option" button can be used. The "Option" pops up the Option dialog box as follows, where users can customize the export data items in the dialog box which are Packet #, Name, TimeStamp, Length and DESCRIBE.

[ Export Packet List...



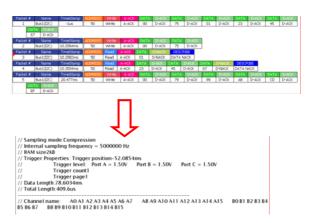
- 1 - 1



Fig 3-11: Option Dialog Box

For instance, all the export options are selected entirely. See the below

picture:





	apture Window	<u>1 X</u>
🛃 Capture Window Ctrl+	Apture to Note: Clipboard Clipboard MsPaint Select Region Select Line Color Color of the Note	
	Capture	Cancel

#### Fig 3-13: Capture Window

This feature is equivalent to [Alt]+[Print Screen], or [Print Screen]

#### Capture to

File – Save the captured image as either a jpeg or bmp Clipboard – Copy the captured image to the clipboard for use in other applications.

MsPaint – Directly start MsPaint to view the captured image.

#### **Capture Region**

Full Screen – Capture everything on the screen. Select Region – After pressing the capture button, a cross-hair will appear on the screen. Left click the mouse button to drag an area to capture. Select Line Color – Click the color box to change the color.

**Opposite of Color** – Click this check box to ensure that the note text will be the opposite of the line color.

Color of the Note- Choose the color of the note text.

Note - Type in a note to attach to the captured image.

Capture – Click the button to capture the image.

Cancel - Click Cancel to end the capture.



	ZEROPLUS Logic Analyzer	×
-	The program needs Do you want to save	to restart. • the current document?
	<u>Y</u> es <u>N</u> o	Cancel

Fig 3-15: When changing languages, the above screen will be displayed and the program will need to be restarted.

5	Print		Ctrl+P	

#### Tip:

Language

This function has been
enhanced; now users can
select the pages which they
want to print or only the
Current Page.

Print		<u>? ×</u>
Printer		
<u>N</u> ame:	\\LUPY_CN\hp LaserJet 100	Properties
Status:	Ready	
Type:	hp LaserJet 1000	
Where:	USB001	
Comment		
Print range		Copies
		Number of <u>c</u> opies: 1
C Pages	from: 1 to: 272	
C Currer	nt Page	1 2 3 3 Collate
		OK Cancel

Fig 3-16: Click to enter the **Print** dialog box.

	Ale Status A Status A Status (Status (Sta
Print Preview	
	Fig 3-17: Click to show a <b>Preview</b> of the <b>Print</b> .
Recent File	Show the recently saved file.
Exit	Exit the program.



## 2. Bus/Signal

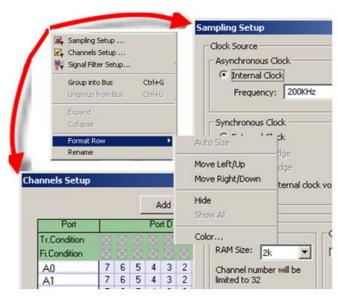


Fig 3-18: Bus/Signal Menu.

	🐢 👯 📲 🔟 🕨	▶ 🔲 2K	💌 👬 👹 🖬 SMHz	• nn nn 50% • 👫 🐳
--	-----------	--------	--------------	-------------------

Fig 3-19: Trigger Tool Box.



#### Menu Bar: Bus/Signal Menu Item Detail Menu & Dialog Box Sampling Setur × Clock Source Asynchronous Clock Internal Clock Frequency: 5MHz • Synchronous Clock 🌉 Sampling Setup ... C External Clock 🙆 Rising Edge 100KH C Falling Edge (Min:0.001Hz, Max:100MHz) Note: The external clock voltage level is the same as the port A trigger level Sampling – – RAM Size Compression Mode Signal Filter RAM Size: 2K 🔽 Data Compression • Channel number will be limited to 24 Restore Defaults ОК Cancel Help Fig 3-20: Sampling Setup See Section 4.1 for detailed instructions. Tip: 2K 50MHz कोंक 🚻 www.ww Icon Description Decrease **₽**II4 Fig3-21: RAM Size RAM Size Increase Choose the RAM Size and the internal clock frequency from I∰I RAM Size the pull-down menus. Decrease Internal лл Clock Frequency Increase Internal າກກາ Clock Frequency RAM Size The amount of the acquired data that can be stored by the Logic Analyzer depends on the amount of the allocated RAM. The total depth of the memory for the LAP-A/C is 128K Bits in each probe. If the Logic Analyzer starts gathering data with a 128K memory range, it will take a long time to find the required information. In order to avoid spending a lot of time gathering data, select a smaller RAM Size. The RAM Size options are 2K, 16K, 32K, 64K, 128K and 256K. So, if gathering data with 128K takes a long time why does 256K make sense? The reason for this extra RAM Size is to cope with the fact that a few of the 1~16 channels may have a large data input. Use the pull-down menu to choose the speed of the clock on Tip: the board being tested. **Clock Source** Asynchronous Clock The sampling frequency should be more than 4 times higher than the signal to be measured so that the waveform duty cycle depiction will be accurate.

FM07I4A

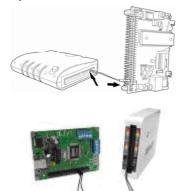
#### Sampling Setup

Clock Source	
-Asynchronous Clo	ck
<ul> <li>Internal Clock</li> </ul>	
Frequency:	100KHz 💌
	100Hz
Synchronous Clock	500Hz 1KHz
C External Clock	5KHz
C Dicipa Edu	25KHz
C Rising Ed	
C Falling Ed	
Note: The exte	200KHz 400KHz
	800KHz
	1MHz
	10MHz
- Sampling	25MHz
RAM Size	50MHz
RAM Size: 16K	80MHz
1 I I I I I I I I I I I I I I I I I I I	100MHz
	150MHz 200MHz
Apply	OK Can

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

Synchronous Clock of LAP-A/C



Tip:

Compression

#### Check the box to compress all the data.

Compression is used to compress acquired data through a lossless compressor. The purpose of this compression is to place more data in a limited memory than in an actual memory. The compression rate of the Logic Analyzer can be up to 255 times. This means that the maximum acquisition can be 32M Bits (128Kx255= 32M Bits) for each channel. The chosen capacity of the memory, 1MB, means that the maximum data being sieved out arrives at 1MB\*255=255M Bits (Per Channel). **Note:** The rate will change depending on the data being analyzed.

Choose the frequency of the clock on the board of the Logic Analyzer. Select "External Clock" to acquire data through external sampling. Choose either "Rising Edge" or "Falling Edge" to execute the analysis process.

According to the users input the value of external frequency in software, the software can count the relevant value about signal mode and frequency. For example: the value of the message, the time scale and the zoom in and out will be the value of time mode.

#### **Connecting the Synchronous Clock**

Use one of the single connecting cables to put one end on the testing board and the other in the LA as shown in the diagram opposite.



Tip:

Signal Filter Setup

		7	6	5	4	3	2	1	0
PortA	Trigger Condition	$\otimes$	$\otimes$	$\otimes$	$\boxtimes$	$\otimes$		$\otimes$	X
	Filter Condition								
PortB	Trigger Condition	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$
rono	Filter Condition								
PortC	Trigger Condition	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$
FUNC	Filter Condition								
PortD	Trigger Condition	$\times$	$\times$	$\boxtimes$	$\boxtimes$	$\times$	$\boxtimes$	$\boxtimes$	$\times$
PonD	Filter Condition								
	y Setup rate Filter Delay								
Select			© s O s	t Delay S itart Edge ind Edge 'eriod#De			Delay Tin 10us (Min:10us (Max:655	)	

Fig 3-22: Signal Filter Setup Dialog Box

The function of Signal Filter is to use an alterable judgment circuit which can filter undesired signals in order to capture and store valuable data in the memory. When the combination of input signals from each channel meets the filter conditions, the section of acquired data will be gathered by the Logic Analyzer and stored in the memory. After storing the data, it will return to the Logic Analyzer's system and be displayed as a waveform. If the combination does not meet the filter conditions, it won't gather and store data.

1. **Don't Care means that the Logic Analyzer** captures all signals from sampling.



Fig 3-23: High and Low Levels

It is the system default.

2. High Level means that the Logic Analyzer captures and displays the input signals satisfying the high level.

3. **EXAMPLE** = Low Level means that the Logic Analyzer captures and displays the input signals satisfying the low level.

#### Tip:

Tip:

Select the Signal Filter Setup from the pull-down menu of the Bus/Signal or click the icon or the Button on the Sampling Setup dialog box to open the Signal Filter Setup dialog box.

There are three modes of Signal Filter

configuration for each channel.



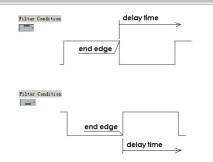


Fig 3-24: High and Low Levels

Signal Filter Delay Setup Filter Delay – According to the filter condition. Start Edge – Show the waveform from the start edge to the delay time interval.

See details in Section 4.1.

🌠 Channels Setup	Part         Part <th< th=""></th<>
Tip:	Fig 3-25: Channels Setup
Channels Setup	See details in Section 4.2.
	Click the Add Bus/Signal button to add a channel. This will
Tip:	appear as ' New0'.
Add Bus/Signal	Click the Bus or channel you want to delete and press the <b>Delete Bus/Signal</b> button.
Delete Bus/Signal	Press the <b>Delete All</b> button to delete all the Buses and channels.
Delete All	Press <b>Restore Defaults</b> to return all channels and Buses to the system defaults.
Restore Defaults	Select this function when adding and deleting channels, the software reserves the original waveform; not select this function, the waveforms in channel are cleaned up.
Group into Bus Ctrl+G	Signals can be grouped into Buses by pressing <b>Ctrl + G</b> . Signals can be added, deleted ,copied and grouped into Bus,
Reserve waveform data and show them	using the mouse or the keyboard, or right click and select the desired operations from the pull-down menu The movement of a signal channel are Auto Size (not available in waveform display), Move Left/Up, Move Right/Down, Hide, Show All and Color)
Ungroup from Bus Ctrl+U	Ungroup signals from Buses by pressing <b>Ctrl + U</b> .
Expand	A Bus contains at least 1 channel. In order to see these channels click the symbol before the name of the Bus. Bus/Signal Bus1 A2 A2 A3 A3 A4 A4 A5 A5 Bus A5 Bu
	▲5 A5 31 ▲6 A6 8



	Fig 3-26: Expand			
	If the Bus has been expanded, or Bus name to <b>Collapse</b> the Bus.	lick the <b>V</b> symbol before the		
	▼ Bus1	- × · × · × · × · · × · · · × · · · · ·		
	• A0 A0			
	•A1 A1	20 20 :		
Collapse	🥑 A2 A2 🕅	40us 40u		
	🧹 <b>A3</b> A3 🛛 🕅	80us		
	✓ A4 A4	160us		
	🖌 A5 A5			
	🥑 A6 A6			
	Fig 3-27:	Collapse		
	Auto Che			
Format Row	Auto Size			
	Move Left Move Righ			
	Hide			
	Show All			
	Color			
Tip:	Fig 3-28: Click to change	the Bus or signal display.		
Format Row	ů ů	0 1 7		
Auto Size ( it is not available in	Change the display of a Bus or a	a signal.		
Waveform Display mode)	Size the signal columns automation	tically.		
Move Left/Up (change to Move Left in				
Listing Display)	Highlight a signal or Bus and clic			
Move Right/Down (change to Move	signal or Bus up (left) through th Highlight a signal or Bus and clic			
Right in Listing Display)	the signal or Bus down (right) the Bus/signal.	-		
Hide	Highlight a signal or Bus and clic	ck <b>Hide</b> to hide it.		
Show All	Click to show all signals and Bus	ses that have been hidden.		
Color	Highlight a signal or Bus and clic	k Color to change the color.		
	Highlight a signal or Bus and clic	k Rename to rename the Bu		
Rename	or signal.	a rename to rename the Du		



### 3. Trigger

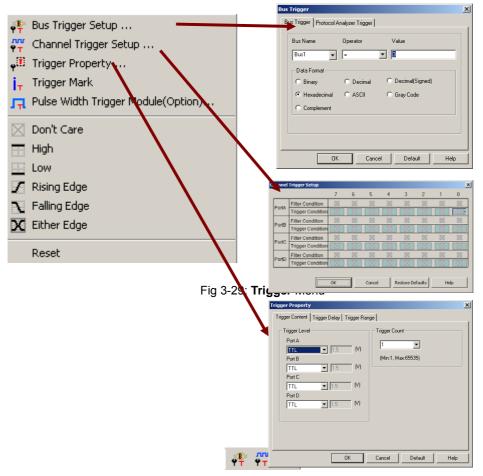


Fig 3-30: Trigger Tool Box



### Menu Bar: Trigger Menu Item

Detail Menu & Dialog Box

	<b>-</b>	
	Bus Trigger Bus Trigger Protocol Analyzer Trigger	×
	Bus Name Operator Value Bus1	
📲 Bus Trigger Setup	Data Format Data Format Binary O Decimal O Decimal(Signed) Hexadecimal O ASCII O Gray Code Complement	
	OK Cancel Default H	lelp

### Fig 3-31: Set Bus Trigger

See Section 4.1 for detailed instructions.

Cha	annel	Trigger Setup								
			7	6	5	4	3	2	1	0
	PortA	Filter Condition	$\otimes$	$\boxtimes$	$\otimes$	$\otimes$	$\otimes$	$\otimes$	$\boxtimes$	$\otimes$
	PUNA	Trigger Condition	$\mathbf{X}$			X				
tup	PortB	Filter Condition	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\boxtimes$	$\times$	$\boxtimes$	X
	one	Trigger Condition								
	Option of	Filter Condition	$\times$	$\boxtimes$	$\times$	$\boxtimes$	$\times$	$\times$	$\boxtimes$	X
P	PortC	Trigger Condition	$\mathbf{X}$							
	lot D	Filter Condition	$\mathbb{X}$	$\boxtimes$	$\times$	$\boxtimes$	$\times$	$\times$	$\boxtimes$	$\times$
F.	IPortD F	Trigger Condition								

Fig 3-32: The trigger action tells the Logic Analyzer when to send data to the PC. The trigger conditions determine when the trigger point starts to record the information.

🖵 Trigger Mark	Open the Trigger Mark function.			
	See Section 4.1 for detailed instructions.			
 규 Pulse Width Trigger Module(Option)	Pulse Width Trigger Module: Set a trigger condition for a single channel, and the signal in this channel can be			
Tip:	triggered in the predetermined range. However, this function is required to use with the hardware of the Pulse			
It is not necessary to register as it can be used for free.	Width Trigger Module. (If you want to learn the detail, please refer to the Specification of the Pulse Width Trigger Module.)			
🔀 Don't Care	Set the trigger condition as " <b>Don't Care</b> " See Section 4.1 for detailed instructions.			
🚟 High	Set the trigger condition as "High"			
	See Section 4.1 for detailed instructions.			
Low	Set the trigger condition as "Low"			
<b></b>	See Section 4.1 for detailed instructions.			
🖌 Rising Edge	Set the trigger condition as "Rising Edge"			
Harris Cago	See Section 4.1 for detailed instructions.			
	Set the trigger condition as "Falling Edge"			
Falling Edge	See Section 4.1 for detailed instructions.			



Edge	Set the trigger condition as " <b>Either Edge</b> " See Section 4.1 for detailed instructions.
	-

Reset

🚚 🅄 Trigger Property ....

Trigger Content Setup

Decrease

position

Description

trigger position

Increase trigger

Trigger Page

Trigger Count

Tip:

lcon

-

4

N/A

N/A

X Either

Reset the trigger condition.

Max 65535)

Fig 3-33: Set Trigger Content

See Section 4.1 for detailed instructions.

The voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep. There are 4 ports available; each port has the ability to assign different voltages to meet the users' requirements. Use the pull-down menu to choose between TTL (default TTL), CMOS (5V), CMOS (3.3V), ECL and User Defined (choose the value of the Trigger Level – 6.0V to 6.0 V).

50% 💌 🤻	⊧ 📲 Page  1	💌 Count	1	•
(1)	(2)		(3)	

Fig 3-34: Trigger Position, Trigger Page, Trigger Count

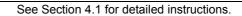
(1) Represents the Trigger Position of a memory page.

- (2) Represents the Trigger Page.
- (3) Represents the Trigger Count.

Tip:		Trigger Property X
т	rigger Delay	Trigger Content Trigger Delay Trigger Range
Icon N/A	Trigger Delay	Image: Page         Image: Page: Page: Page         Image: Page:
		the view.     OK     Cancel     Default     Help       Fig 3-35: Set Trigger Delay

### Trigger Level





Trigger Delay	10us
---------------	------

Fig 3-36: Set up Trigger Delay clock under time display.

Trigger Delay 1000

Fig 3-37: Set up **Trigger Delay** clock under sampling site display.

The **Trigger Delay** setting in **Tool Box** equals to that in the above dialog box.

Tip:			Trigger Property	×
	Tri	gger Range	Trigger Content   Trigger Delay   Trigger Range	
-	lcon	Description	Range Setting	
_	N/A	Trigger Range		
			Time Sample 🔽 1 minute 💌	
			OK Cancel Default Help	
			Fig 3-38: Set Trigger Range	

### 4. Run/Stop



Fig 3-39: Run/Stop Menu



Fig 3-40: Run/Stop Tool Box



## Menu Bar: Run/Stop

Menu Item		Detail Menu & Dialog Box
Single Run	F5	Click to run once. See Section 4.1 for detailed instructions.
Repetitive Run	F6	Click to run continuously until the <b>Stop</b> button is pressed. See Section 4.1 for detailed instructions.
Stop	F7	Click to stop the repetitive run. See Section 4.1 for detailed instructions.

### 5. Data

	an Analytic Range					
<b>T</b>	Filter					
🔯 Bus W	idth Filter					
Data (	Iontrast					
👪 Find D	ata Value	Ctrl+F				
💻 Find P	ulse Width					
] 🔶 To the	Previous Edge	F11				
♦] To the	Next Edge	F12				
Go To		•	<b>T</b> ≹ Ba⊨	Go To T Bar	Т	
🐈 Add B	ar	Alt+A	A K	Go To A Bar	А	
<mark>-2</mark> Delete <sup>Bar</sup>	Bar	Alt+B	В⊻ Ван	Go To B Bar	В	
🛐 Zoom		E		Go To More		
🤭 Hand		Н	-			
📐 Norma	al	ESCAPE		Binary		
Toom	In	F9		Decimal		
		F8		Decimal (Sign	ued)	
	all Data	F10	✓	Hexadecimal		
	us Zoom	Ctrl+Z		ASCII		
		Cuitt2		Gray Code		
Data P	format	•		Complement		
Wavef	orm Mode	Þ	✓	Square Wavefo	orm	
List Da	ita Mode	•		Sawtooth Wav	eform	
			~	All Data		
				Sampling Chan	ged Dot((	Compression)
				Data Changed	Dot(Com	pression)
		Fig 3-41: <b>[</b>	) oto			
		EIU 3-41	лата	IVIETU		

Fig 3-41: Data Menu





📩 Bus Width Filter...

### Menu Bar: Data

Menu Item	Detail Menu & Dialog Box				
Select an Analytic Range	Check the box to enable the Analytic Range to be changed by dragging the Ds and Dp bars with the left mouse button.				
	Noise Filter: It can filter 0~10 Clock's positive pulse				
	width or negative pulse width sigr	nal.			
	Noise Filter	×			
🚋 Noise Filter	Noise Filter: None				
	ОК	Cancel			
	Fig3-43: Noise Filt	er			

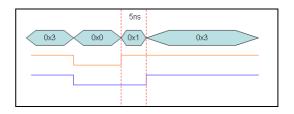
See Section 4.8 for detailed instructions.

Bus Width Filter			×
Bus Width Filter	1		
ОК		Cancel	

Fig3-44: Bus Width Filter

Select the check box to activate the function of the Bus Width Filter in the dialog box, and then users can input the corresponding value of the width to be filtered in the right edit box. Input the time value of the width when the display is in the Time Display or the Frequency Display, and the unit is based on time, such as s, ms, us, etc.; if the inputted value is out of the range, it will switch to the best time value in range. Input the clock value of the width when the display is in the Sampling Site Display, and the range of the input is from 1 to 65535.

For example, after activating this function, and then input the value, 5ns. The Bus Data which is less than or equal to 5ns will be filtered as the figure below:





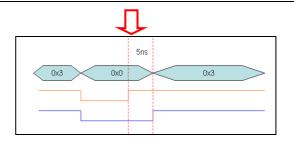


Fig3-45: Before and After Filtering

	Data Contrast Settings  Activate Data Contrast Contrast Files Basic File LaDoc1 Contrast File LaDoc1		× •
	Contrast Beginning Point T Bar Beginning of Data	Error Tolerano	v.
	Contrast Result		Error Stat.
Data Contrast	Roll the contrast waveforms synch Display files the contrast difference Display files horizontal	es ·	Pin Assignment Perform Contrast e Help
	Fig3-46: Data	Contrast	

Data Contrast: It is used to contrast the difference for the two files of the same style. One is the Basic File, and the other is the Contrast File. The contrast file can display the difference between the Basic File and the Contrast File.

		Waveform-Find			×
👪 Find Data Value	Ctrl+F	Activate the fun Bus/Signal Name: Bus Item: Start Start At: Ds	Find:		vious Close Max Value: F Statistics Statistics 0
		Fia 3-47: W	aveform-Fin	d Dialog Box v	without Activate

the Function of Chain-Data-Find Use the pull-down menu to select the Bus/ Signal Name:

The list of Find depends on whether it is a Bus or Signal that is being searched in:

Bus – Choose among =, !=, In Range and Not In
Range (enter the value for Min Value and Max Value).
Signal – Choose among Rising Edge, Falling Edge,
Either Edge, High and Low.

**Start At** - Choose the position to start our search by selecting one of the following:

Ds, T, A, B, ect. (select from the pull-down menu). When Found - Choose A, B or other bars to mark the

position where it is coincident with the set conditions. **Statistics** – Show the number of instances of the search results.

Note: It is available only when searching through a Bus.

Waveform-Find	1			×
🔽 Activate the	function of Chain-	-Data-Find		
Bus/Signal Name	e <b>:</b>			
Bus1		▼ Next	Previous Close	
example,0X32,0	X45,0X50,0X66. I	a comma to compart th It needs to add the pa 0X2A, DATA:0X20.	nem, for cket name in the Protocol	_
				- 1
Start At:	End At:	When Found:	- Statistics	
Ds	▼ Dp	▼ A	▼ Statistics	
			0	

Fig3-48: Waveform-Find Dialog Box with Activate the Function of Chain-Data-Find

### Tip:

The function of Chain-Data-Find is mainly for finding the data in the packets of Bus and Protocol Analyzer which have some serial data. For example, it can start finding with the serial packet segments (there are 0X01, 0X02 and 0X03) in the Bus. It improves the efficiency of Data Find. See the following process:

### Tip:

Remember the final conditions: When the find function is used, the function of displaying the final conditions is added. When you have closed the Waveform-Find dialog box, and you want to find the set conditions, you can open the Waveform-Find dialog box again for the system has saved the last set conditions.



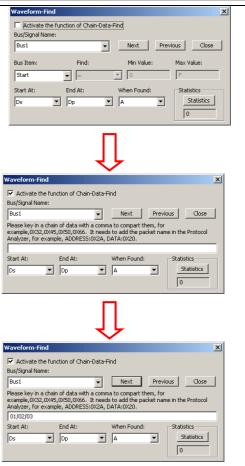


Fig 3-49: Process of Activating the Function of

Chain-Data-Find

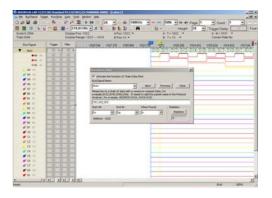
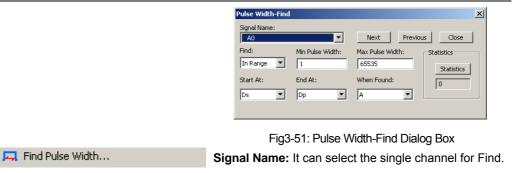


Fig3-50: Function of Chain-Data-Find Displayed on

the Waveform Window



Find: It can select the Find conditions which are "In

This function is mainly used for finding

the pulse width in a single channel and the single channel of a Bus. It improves

the efficiency of finding the Pulse Width

for engineers and strengthens the Find

function of the Logic Analyzer.

Tip:

Range", "Min Value", ">", "<" and "=". When users select the option of "In Range", they can input the value of the Min Pulse Width and Max Pulse Width between 1 and 65535 and find the Pulse Width in range. When users select the "Min Value", they can find the Min Pulse Width for the present single channel. When users select the options ">", "<" and "=", they can input the value of the Pulse Width between 1 and 65535 and find the Pulse Width in range.

**Start At:** Select the Start point of Find. The selectable items are all Bars; the default is the Ds Bar.

**End At:** Select the End point of Find. The selectable items are all Bars; the default is the Dp Bar.

When Found: Select a Bar to mark the found Pulse Width. The selectable items are all Bars; the default is A Bar.

**Statistics:** It can count the number of Pulse Width in the present range.

Next: It can find the next Pulse Width.

Previous: It can find the previous Pulse Width.

For example: Find in the A1 channel; the Pulse Width is equal to "20us"; take the A Bar as the mark. See the below figure:

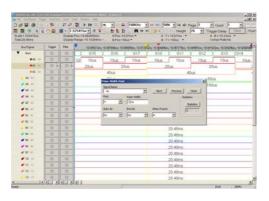


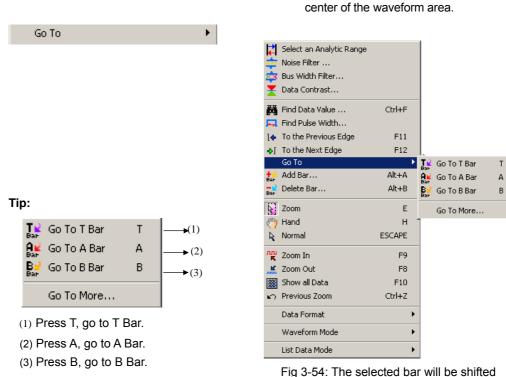
Fig 3-52: Pulse Width-Find on the Waveform Window

14 To the Previous Edge	F11	Go to the previous edge sweep of the indicated signal.
♦] To the Next Edge	F12	Go to the next edge sweep of the indicated signal.
		Go To T, A, B, or Go To More
		380.007         -145.002         -145.002         -104.002         -200.007         -752.016           201.400

Fig 3-53: Go To T Bar: T Bar will be displayed in the

### FM07I4A





to the center of the waveform area.

<mark>+</mark> ≧ Ba⊨	Add Bar	Alt+A

Add user defined bars.

- 1. Click the above menu item from **Data** menu, or click **Add Bar** icon from **Tool Bar**.
- 2. Give a **Bar Name**, define a **Bar Color**, and set a **Bar Posi**tion.
- 3. Define the **Bar Key** with the number between 0 and 9.

#### Tip:

The number shortcut is set in the Add Bar dialog box. Every new bar can be filled in one number which is used to find the required bar faster; the default number of the new bar is 0. It is noticed that once the number key is set, it can't be modified, and each new bar can named with the same number, that is to say, one number can name many bars.

For example, users can set the number 3 as the shortcut key. When users press the number 3 key, the C Bar will be displayed in the centre position of the screen.





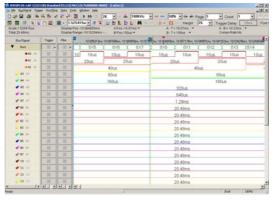


Fig3-56: Add a Bar with the number between 0 and 9



🔫 Delete Bar...

Alt+B

Delete a user defined bar.

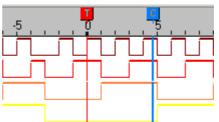
- 1. Click the above menu item from **Data** menu, or click **Delete Bar** icon from **Tool Bar**.
- 2. Select a user defined bar, and click

on Delete.

3. Delete the selected Bar with the **Delete** key on the **Keyboard.** Use the mouse to select the added bar and press the **Delete** key on the keyboard to delete the bar.

Delete Bar		×
C	Delete	
	Close	

Fig3-57: Delete Bar Dialog Box



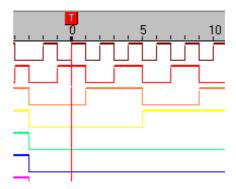


Fig 3-58: Delete a selected Bar.

E 200m E

#### Tip:

A Zoom-In or a Zoom-Out view will be centered in the Waveform Display Area, and the new zoomed view will be sized according to the available space on the display.

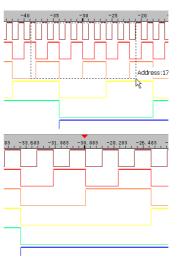


Fig 3-59: To Zoom In, left click and drag



the mouse/point from left to right.

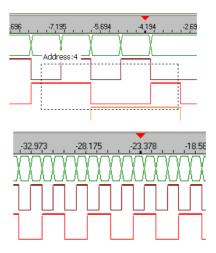
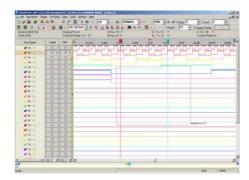


Fig 3-60: To **Zoom Out**, left click and drag the mouse/point from right to left.



When users activate the **Zoom** to zoom in / zoom out the selected area, the Tooltip on the right corner of the bottom will display the Time, Clock or Address of the selected area. When selecting the Zoom function, and users are pressing and dragging the left key, the information on the right corner of the bottom will be changed and updated with the width of the selected area. And the information is displayed on the right corner of the bottom in the way of Tooltip. When users loosen the mouse, the information will disappear.

#### Tooltip:

Time/Frequency Sample: xxx (time)

/ns (unit)

Address: xxx (There is no unit with the

address.)

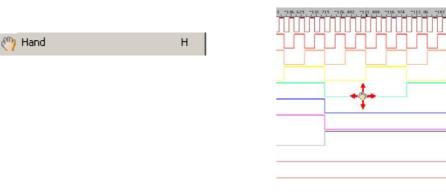


Fig 3-62: Click **Hand**, and then depress and hold the left mouse button to drag.

Fig 3-61: To display the Tooltip, left click and drag the mouse/point from right to left or from left to right.



 Normal
 ESCAPE
 Reset the mouse function to the system default.

 Image: State of the system default
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the syst

### Tip:

Zoom In and Out can be switched by changing the percentage value in the pull-down list.

1. The system can set the value of Zoom In and Out:

The default unit is µs. When zooming in, it will be automatically changed to ns. When zooming out, it will be changed to ms, s or ks.

2. Pull-down Menu:

There are thirty scales. The maximum zoom in and out is the cycle of each grid, 0.0001piece. The minimum zoom in and out is the cycle of each grid, 1,000,000,000.

Zoom in and out (the proportion): with each grid being the cycle, the zoom in and out (%) is 100%. The time of Zoom In and Out counts by the clock of each grid (sample frequency). For example:

(1) Each grid is being a cycle; the zoom in and out is 100%. The time of Zoom In and Out will be presented by the clock of each grid X (1/sample frequency).

(2) Each grid stands for the clock of 100 pieces, the zoom in and out is 1% and the time of Zoom In and Out will be displayed by the cycle of each grid X (1/sample frequency).

Display Pos:0 Display Range:-250 ~ 25



Fig 3-64: Result from Normal to Zoom In

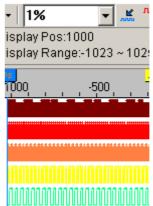


Fig 3-65: Result from Normal to Zoom Out

FM07I4A



🗱 Show all Data	F10	
		Fig 3-66: Show all Data
🖍 Previous Zoom	Ctrl+Z	Return to the last zoom.
		Binary Decimal Decimal(Signed)

×

Data Format

Complement Fig3-67: Data Format

ASCII Gray Code

Show numerical information in Binary, Decimal,

Decimal(signed), Hexadecimal, ASCII, Gray Code, or

Complement.



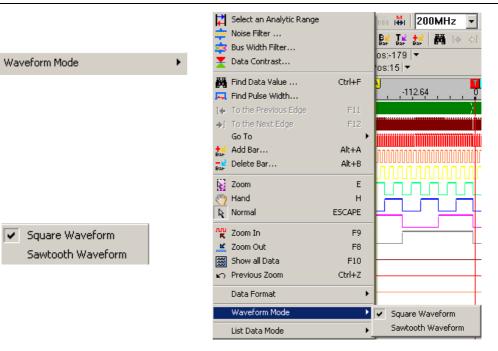


Fig 3-68: Square Waveform

<b>H</b>	Select an Analytic Range		
a a a a a a a a a a a a a a a a a a a	Noise Filter		B⊻ T¥ +2 ∰ l♦ ¢j
28	Bus Width Filter		
Ŧ	Data Contrast		os:-179 ▼
			_'os:15   ▼
69	Find Data Value	Ctrl+F	20.10
<b>–</b>	Find Pulse Width		28.16
14	To the Previous Edge	F11	
¢٦	To the Next Edge	F12	
	Go To	•	000000000000000000000000000000000000000
+ 2 Bat	Add Bar	Alt+A	
Bar Bar	Delete Bar	Alt+B	
Bar			
	Zoom	E	
3	Hand	Н	
R	Normal	ESCAPE	
ĸ	Zoom In	F9	
<b></b>	Zoom Out	F8	
	Show all Data	F10	
ĸ)	Previous Zoom	Ctrl+Z	
	Data Format		-
	Data Format		
	Waveform Mode	► F	Square Waveform
	List Data Mode	•	Sawtooth Waveform

Fig 3-69: Sawtooth Waveform



List Data Mode

### Tip:

The data for list mode are so many, to be convenient for users, that there is adding a List Data Mode function. The formats for the List Data Mode are All Data, Sampling Changed Dot (Compression) and Data Changed Dot (Compression).

۲

All Data: It is the present display mode.

### Sampling Changed Dot

(Compression): Take the sampling changed dot as the compression data reference dot.

**Data Changed Dot (Compression)**: Take the present data change dot as the compression data reference dot.

	Select an Analytic Range		Þ	∳ I∯	1 2	00M	Hz	•	n vu	nur	50
-	Noise Filter		B	🖌 Tı	d <mark>∔</mark> de	M	14		8	•	80
	Bus Width Filter		05	s:-178	8 🔻					Α-	Т
*	Data Contrast		0:	s:15	•					В-	Т
两	Find Data Value	Ctrl+F		B1	B2	B3	В4	B5	B6	B7	1
н,	Find Pulse Width		ř								
l+	To the Previous Edge	F11	L							Ť	
•[	To the Next Edge	F12									
	Go To	+	H	0	0	0	0		0	0	
<b>+</b> ∠ Ba⊦	Add Bar	Alt+A	Þ	0	0	0	0	0	0	0	
Bar	Delete Bar	Alt+B	Þ	0	0	0	0	0	0	0	
	Zoom	E	b	0	0	0	0	0	0	0	
3	Hand	н	k.	0	0	0	0	n	n	0	h
R	Normal	ESCAPE		0	0	0	0	n n	0	0	
ллі K	Zoom In	F9		0		0	0	n n	0	0	
1	Zoom Out	F8	Ľ					Ľ			
	Show all Data	F10	ŀ	0	0	0	0	0	0	0	
K)	Previous Zoom	Ctrl+Z	ŀ	0	0	0	0	0	0	0	
	Data Format	•	ŀ	0	0	0	0	0	0	0	
	Waveform Mode	•		0	0	0	0	0	0	0	
	List Data Mode	Þ		All (	Data						
	1 1 0 0 0			San	npling	Chan	ged D	ot(Co	mpres	sion)	
	0 0 1 0 0			Dat	a Cha	naed	Dot(C	omor	ession	ù l	

Fig 3-70: List Data Mode: All Data, Sampling Changed Dot (Compression) and Data Changed Dot (Compression).



Customize ...
Color Setting .

Bus Property ... Refresh Protoco Multi-stacked Lo Analog Wavefor DSO-stacked Se ×

--

elp

### 6. Tools

	Customize
	Common Setup   Toolbars   Shortcut Key   Auto Save
l Analyzer	⊢ Waveform Display Mode
gic Analyzer Settings m	C Sampling Site Display C Frequency Display
ttings	Time Display     C Hide time of waveform
	Ruler Mode
	C Regular Ruler Waveform Height 26
	Time/Sampling Site Ruler     Font Size
	Correlated Setting
	Auto-Close Dpen/Close Compression Warning
	Show Gridline Show the T Bar in the middle area
	Show Tooltip 🔲 Open/Close Double Warning
	When the roller is moved toward back, the Time Axis in the waveform area will move toward right.
	Data Process
	What do you want to show when you press the Stop during the running?
	• Keep the Present Data C Read the Captured Data
	Check for Update Bestore Defaul
	OK Cancel H

Fig 3-71: Tools Menu



Fig 3-72: Show Time/Height Tool Box



### Menu Bar: Tools

Menu Item	Detail Menu & Dialog Box
	Customize
	Common Setup   Toolbars   Shortcut Key   Auto Save
	Waveform Display Mode
Customize	Sampling Site Display     Frequency Display
	C Time Display C Hide time of waveform
	Ruler Mode Waveform Setting
	Regular Ruler     Waveform Height 22
	C Time/Sampling Site Ruler
	Correlated Setting         Image: Correlated Setting
	<ul> <li>Show Tooltip Ø Open/Close Double Warning</li> <li>When the roller is moved toward back, the Time Axis in the waveform area will move toward right.</li> </ul>
	Data Process What do you want to show when you press the Stop during the running? C Keep the Present Data
	Check for Update Restore Defaults
	OK Cancel Help
	Fig 3-73: <b>Customize</b> Dialog box
	See Section 3.4 for detailed instructions.
	Customize X
	Common Setup Toolbars Shortcut Key Auto Save
	Toolbars
	☑Run/Stop
	☑ Display Mode
	✓Windows ✓Mouse Pattern
	Zoom
	In the second s
	✓ Data Contrast/Screen Display
	OK Cancel Help
	Fig 3-74: <b>Toolbars</b> Setting



Customize		×
Common Setup   Toolbars   S	Shortcut Key Auto Save	
Commands:	Current Keys:	
Add Bar Capture Window Close Delete Bar	Alt+A	Assign Remove
Down End Esc Export Waveform F2 F3 Find Data Maha	1	Reset All
Currently affected to :	Select New Shortcut Key:	
Description: 井≧ Add Bar ₿ан		
	OK Cancel	Help

Fig 3-75: Shortcut Key Setting

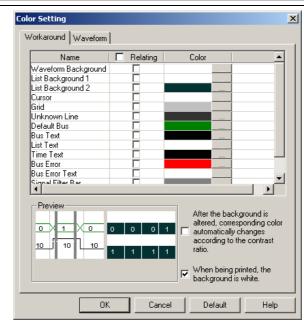
Customize 🔀
Common Setup Toolbars Shortcut Key Auto Save
Activate
File Name: LA
Save Path Name:
D:\Documents and Settings\123\My Documents\LA
Repetitive Run Time Interval:  Data Display Menu Renewal Mode  Every Renewal  Open the first file after stopping the Run
Default
OK Cancel Help

Fig 3-76: Auto Save Setting

See Section 3.5 for detailed instructions.



×



### Tolor Setting ...

BUS

### Fig 3-77: Color Setting

See Section 3.6 for detailed instructions.

	Bus Setting	
	C Bus	Color Config
	C Activate the Latch Function	A0 👻
		Rising Edge
Due Duese subs	Protocol Analyzer Setting	
Bus Property	Protocol Analyzer	Parameters Config
	C ZEROPLUS LA 1-WIRE MODULE V1.10.	00(CN01)
	C ZEROPLUS LA 3-WIRE MODULE V1.04.	
	<ul> <li>ZEROPLUS LA AC97 MODULE V1.02.00</li> <li>ZEROPLUS LA ARITHMETICAL LOGIC N</li> </ul>	
	C ZEROPLUS LA BUS MODULE V1.00.00(	
	C ZEROPLUS LA CAN 2.0B MODULE V1.3	2.00(CN01)
	C ZEROPLUS LA CCIR656 MODULE V1.33	
	C ZEROPLUS LA Compact Flash 4.1 MOD	
	Use the DsDp	Find
	More Protocol Analyzer	
		OK Cancel Help
	Fig 3-78: <b>B</b>	us Property
	Bus: Activate the function of a	nalyzing the Bus.
See Section 4.5 for detailed	Color Configuration: Open the box to set the conditions for the condit	0
instructions.	Activate the Latch Function:	Activate the latch function.
	Protocol Analyzer: Activate the Protocol Analyzer.	ne function of analyzing the
	<b>Use the DsDp</b> : Use the Ds an Protocol Analyzer.	d Dp to help analyze the

Bus Propert

**Find:** Find the desired Protocol Analyzer module. Users can input the Protocol Analyzer name to quickly find the Protocol Analyzer module from many Protocol Analyzers. After inputting the first character of the name in the Find box of Bus Property dialog box, the corresponding module will be displayed in the Protocol Analyzer list box according to the input character. See the figure below:



s Property	<u>&lt;</u>
Bus Setting	
C Bus	Color Config
Activate the Latch Function	AO
	Rising Edge
Protocol Analyzer Setting	
. 2	
Protocol Analyzer	Parameters Config
C ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN	01)
C ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN	·
C ZEROPLUS LA AC97 MODULE V1.02.00(CN01	·
<ul> <li>ZEROPLUS LA ARITHMETICAL LOGIC MODUL</li> <li>ZEROPLUS LA BUS MODULE V1.00.00(CN01)</li> </ul>	E V1.51.00(CN01)
<ul> <li>ZEROPLUS LA BUS MODULE VI.00.00(CN01)</li> <li>ZEROPLUS LA CAN 2.0B MODULE VI.32.00(CN01)</li> </ul>	101)
C ZEROPLUS LA CAN 2.05 MODULE V1.32.00(C)	
C ZEROPLUS LA Compact Flash 4.1 MODULE VI	
ZEROPLUS LA CMOS IMAGE MODULE V1.00.0	
© ZEROPLUS LA CMOS IMAGE MODULE V1.00.0	

Fig 3-79: Find Editor Box

When you input "I" in the Find editor box, the Protocol Analyzer list displays all Protocol Analyzers with the initial character of "I"; see the below picture:

Bus Setting	Color Config
C Bus	Color Conrig
Activate the Latch Function	AO
	Rising Edge
Protocol Analyzer Setting	
Protocol Analyzer	Parameters Config
C ZEROPLUS LA I2C(EEPROM 24LC361/24 ⊂ ZEROPLUS LA I2C(EEPROM 24L) MODUL ⊂ ZEROPLUS LA I2C MODULE V2.02.00(C1 ⊂ ZEROPLUS LA I2S MODULE V1.13.00(C1 ⊂ ZEROPLUS LA ISO7816 UART MODULE V1.13.00(C1)	LE V1.31.00(CN01) N01) N01)
© ZEROPLUS LA IZC(EEPROM 24L) MODUL © ZEROPLUS LA IZC MODULE V2.02.00(CI © ZEROPLUS LA IZS MODULE V1.13.00(CI	LE V1.31.00(CN01) N01) N01)
C ZEROPLUS LA I2C(EEPROM 24L) MODUL C ZEROPLUS LA I2C MODULE V2.02.00(CT C ZEROPLUS LA I2S MODULE V1.13.00(CF C ZEROPLUS LA ISO7816 UART MODULE V	LE V1.31.00(CN01) N01) N01)
<ul> <li>○ ZEROPLUS LA I2C(EEPROM 24L) MODUL</li> <li>○ ZEROPLUS LA I2C MODULE V2.02.00(CI</li> <li>○ ZEROPLUS LA I2S MODULE V1.13.00(CI</li> </ul>	E V1.51.00(CN01) N01) N01) V1.02.00(CN01)

	Refresh Protocol Analyzer data.
🍓 Refresh Protocol Analyzer	Refresh Flotocol Analyzer uala.
L.	
	See Section 4.10 for detailed instructions.

	Multi-stacked Logic Analyzer Settings	×
	Ctivate Stack	
	Stack Type	
	<ul> <li>Memory Stack</li> </ul>	
	C Channel Stack	
	Please select the Logic Analyzer for stacking	
	M1 S/N:000000-0000	
	M2 S/N:000000-0000	
lti-stacked Logic Analyzer Settings	□M3 S/N:000000-0000	
	Synchronous Channel	
	AO	
	Synchronous Trigger Condition	
	Rising Edge	
	OK Cancel H	lelp

Fig 3-81: Multi-stacked Logic Analyzer Settings Dialog Box See Section 4.12 for detailed instructions.

# Analog Waveform

۲

M Single Analog Display	
🔛 Mixed Analog Display	

### Tip:

Mu

When the function of Analog Waveform is activated, the Analog Waveform will be displayed in the waveform area of the Bus's sub-channel and take the space of four channels. And four sub- channels won't draw the waveform. It notes that the sub-channel of the Bus must be more than four channels.

#### **Analog Waveform**

The function of Analog Waveform means that the Display Mode of Bus Data is not the Pure Data Mode, while it displays data change with the curve which looks like a waveform, which, in fact, is a curve to describe the data change. So it is called the Analog Waveform.

The Analog Waveform can be divided into two kinds, namely, Single Analog Display and Mixed Analog Display, see the figures as below:

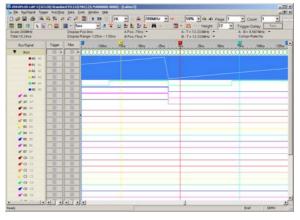


Fig 3-82: Single Analog Display



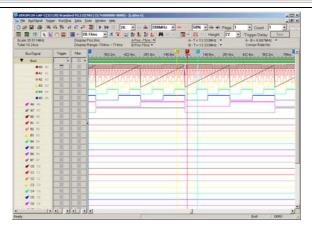


Fig 3-83: Mixed Analog Display

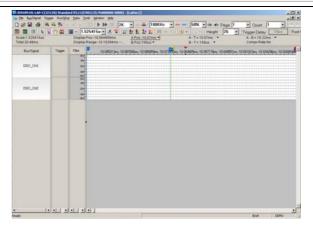
SO-stacked Settings	×
Channel V/Div Setting	
DSO_CH1 V/Div: 2V/Div V	DSO_CH2 V/Div: 2V/Div 🔻
DSO_CH3 V/Div: 2V/Div	DSO_CH4 V/Div: 2V/Div 💌
Channel Setting	
Only display DSO	
DSO_CH1 DSO_CH2	DSO_CH3 DSO_CH4
Channel Height Setting	
DSO_CH1 Height: 80	DSO CH2 Height: 80
DSO_CH3 Height: 80	DSO_CH4 Height: 80
DSO Settings OK	Cancel Default Help

**Channel V/Div Setting:** Users can select the Options, 3V/Div,2V/Div, 1V/Div, 500mV/Div, 200mV/Div, 100mV/Div, 50mV/Div,20mV/Div, 5mV/Div and 2mV/Div.

**Channel Setting:** Users can set the DS0\_CH1, DS0\_CH2, DS0\_CH2, DS0\_CH4, the captured waveform will be displayed on the LA Software; meanwhile, the color of CH can be changed. When selecting the item, Only display DSO, only the activated DSO CH can be displayed on the waveform. The A0~A7 can't be displayed, see as below figure.

DSO-stacked Settings...





**Channel Height Setting:** Set it from 30 to 400. DSO Settings: when the button is pressed, the below box will be displayed.

- ·		
○ TCP/IP	O AUTO	
	]	
	Hz	
	Ps	
	%	
7		۷
<b>v</b>		
7		
<b>T</b>		ns
	· · ·	Hz Ps

**Oscilloscope Brand:** User can select the oscilloscope brand to stack, such as Tektronix. Then click the Online button to show the oscilloscope model, None will be displayed if no oscilloscope is connected.

**Online Mode:** Users can select USB, TCP/IP or Auto. If selecting the USB, the oscilloscope will connect with the PC by USB. If selecting the TCP/IP, the oscilloscope will connect the PC by TCP/IP, and the IP needs to be set the same as the IP of current



PC. If selecting the Auto, users can connect without any setting.

**Current Online Model:** Display the oscilloscope's name.

Sampling Frequency: It matches with the sec/case spin button of oscilloscope. Its value is the reciprocal of horizontal scale, the range is 1/5ns ~ 1/50s.
Stacking Delay: It is used to align the T Bar and the

T Bar of LA when users use the main program to show the oscilloscope's waveform. The range is -1000000ps~+1000000ps.

**Trigger Position:** It matches the horizontal spin button of oscilloscope, the range is 0~100%.

Trigger Channel: It matches the trigger level spinbutton of oscilloscope, the lever range is -16V~ 16V.Trigger Type: The other options is available only

after the active option is selected.

A. Trigger Edge: Users can select Rising Edge or Falling Edge.

B. Pulse: Users can select <, >, =, !=; the range is 33ns~10s.

C. Video: Users can select Line, All Lines, Odd Field, Even Field and All Field.

**Online:** Click the Online to link with the oscilloscope, and the Online button will change into Disconnect button.

Users can set the oscilloscope by selecting the options and inputting values, then pressing OK.

Note: the Stacking Delay is set into the main program. If no oscilloscope is connected or the oscilloscope disconnects, the whole options under the Stack Parameters are unable.

For the above details, please refer to the 4.13.



### 7. Window

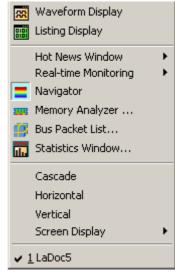


Fig 3-84: Window Menu



Fig 3-85: Window Tool Box

Menu Item	Detail Menu & Dialog Box				
	🏂 File Bus/Signal Trigg	er Run/ <u>S</u> top	) <u>D</u> ata <u>T</u> ools		
	🗋 🖻 📕 🎒 🔍	🖉 🖗 🛹	🕂 🖓 🖓	🙀 🙀 Waveform Display	👪   200
	🕅 📰 🎁 🔖 🕅	۵ 🖑	💥 🕶 5ns	Listing Display	T¥ +2 Bar Bar
	Scale:200MHz		Display Pos	Hot News Window	-75ns 🔻
	Total:10.24us		Display Rar		:75ns 🔻
	Bus/Signal	Trigger	Filter	Memory Analyzer	50
🗝 Waveform Display	A0 A0			Bus Packet List	-50ns
	A0 A0			Statistics Window	H 나 H
	-			Cascade	
	<b>A2</b> A2			Horizontal	
	🧹 A3 A3			Vertical	
	✓ A4 A4			Screen Display	L
	✓ A5 A5	N		✓ 1 LaDoc5	
	<b>~ A6</b> A6				1
	✓ A7 A7				
	<b>60</b> B0				
	<b>61</b> B1	$\square$			



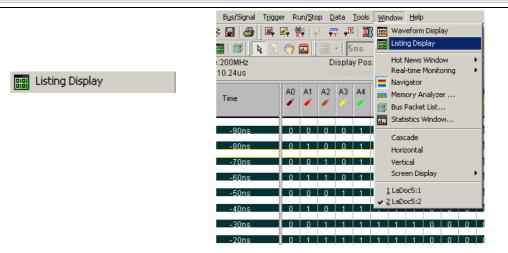


Fig 3-87: Display Signals in Listing.

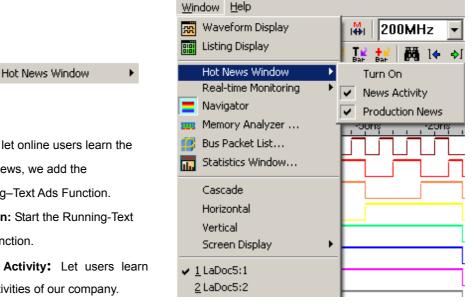


Fig 3-88: Hot News Window and the Pull-down Menu

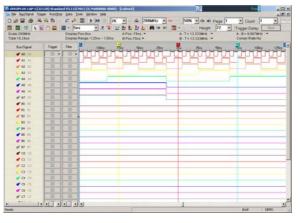


Fig 3-89: Display Hot News Window on the Software

Interface.

rotocol Analyzer MVB\_V1.01.00 Publish

Fig 3-90: Running-Text Ads Interface

#### Tip:

To let online users learn the latest news, we add the Running-Text Ads Function. Turn On: Start the Running-Text

Ads function.

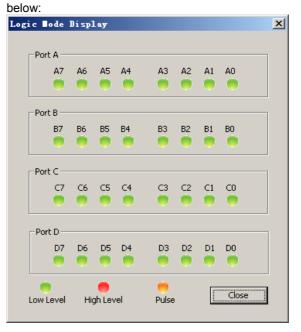
News Activity: Let users learn the activities of our company.

Production News: Let users learn the latest products of our company.

#### Note:

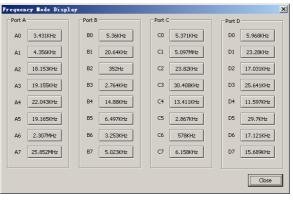
If both News Activity and Production News are turned on. The Running-Text Ads will play News Activity prior to Production News, and play the news in order; the whole process plays repetitively.

Real-time Monitoring: The Level and the Frequency of all the channels can be monitored according to the Real-time Monitoring function of software, which is convenient for users to know the current data status of each channel. There are two display mode, see as

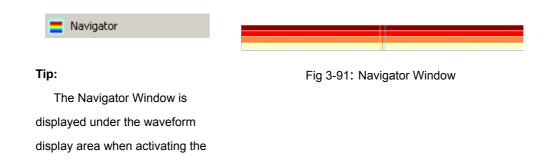


Real-time Monitoring

#### Logic Mode Display



**Frequency Mode Display** 



Logic Analyzer. The Navigator displays the waveform length of all the captured data; it only can display the waveform of the data of four channels. In the Navigator Window, users can click the Left Key of the mouse to select the waveform randomly. The selected waveform keeps pace with the waveform in the waveform display area. The size of the selection frame is in inverse proportion to the Zoom Rate; the larger the Zoom Rate is, the smaller the size of the selection frame is. Users can also click the Right Key of the mouse to select the displayed channel.

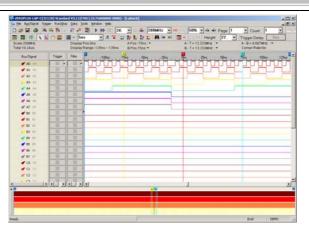


Fig 3-92: Navigator Window under the waveform

display area





Fig3-93: Blue Frame in the Navigator Window

There is a blue frame in the above Navigator Window. Users can click the Left Key of the mouse to select the waveform randomly.

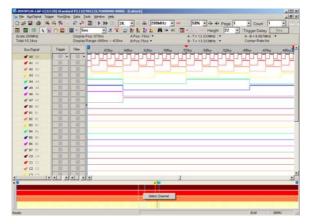


Fig3-94: Select Channel button After clicking the Right Key of the mouse, the Select Channel dialog box will pop up as below.



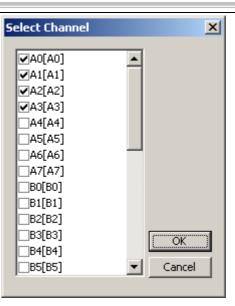


Fig3-95: Select Channel dialog box

In the Select Channel dialog box, users can select the channel which users want to display; users can select four channels at most; the defaulted channels are A0, A1, A2 and A3 (there are four channels in total).



Fig 3-96: **Memory Analyzer** Interface See Section 4.11 for detailed instructions.

🚦 Bus Packet List...

Tip:

Setting: Set up the packet list. Refresh: Click it, the content in the packet list will be refreshed.

Export: Users can use the

fragment to work, record and

analyze the packet list data. As

Export, according to the packet list arrangement, it exports the text file and csv file.

Synch Parameter: Open the Synch Parameter Setting dialog box.

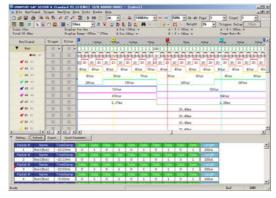


Fig3-97: Display Packet List



Statistics Window	Convert Selection         Conduct Image
	Fig3-98: Statistics Window
	See Section 3.3 for detailed instructions.
Cascade	
	Fig 3-99: <b>Cascade</b> Workspace(s)
Horizontal	<image/>
Vertical	
	Fig 3-101: Align Workspace(s) Vertically



### Screen Display:

	Screen Display	►
	Double Screen Display	
	First Screen Display	
5	Second Screen Display	

When there are two displayers connecting, users can select
🛃, Double Screen Display, to display waveforms on both
two displayers; it is convenient for displaying more
waveforms. 💽, First Screen Display, or 💽, Second
Screen Display, can also be selected to display waveforms
on the first displayer or the second displayer.

### 8. Help

	Logic Analyzer Help	F1
	Keyboard Map	
	Problem Feedback	
ଂ	About ZEROPLUS Logic Analyzer	
	About ZEROPLUS More Protocol Analyzer	

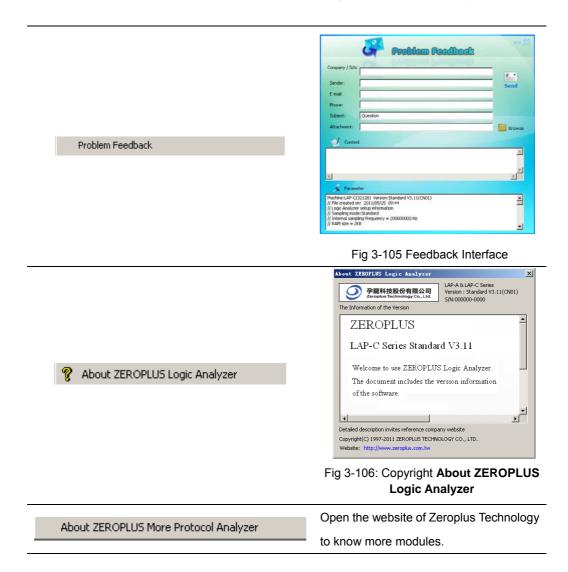
Fig 3-102: Help Menu

### Menu Bar: Help

Menu Item		Detail Menu & Dialog Box		
Logic Analyzer Help	F1	Detect Jame   Secol		LUS
		<ul> <li>I team of Street (cap tright)</li> <li>I team of Street (cap tright)</li> <li>I team of team of</li></ul>	使用手冊	Logie C User Manual
				Traffures
				To stall attace
		Fig 3-103: Op	en <b>Log</b> file.	ic Analyzer H
		Fig 3-103: Op		ic Analyzer H
		Fig 3-103: Op	file.	ic Analyzer H
		Fig 3-103: Op	file.	ic Analyzer H
		Fig 3-103: Op	file.	ic Analyzer H
Variational Mark		Fig 3-103: Op	file.	ic Analyzer H
Keyboard Map		Fig 3-103: Op	file. Hotkey A B T E H Crd+A	ic Analyzer H More waveform to where takes. More waveform to where takes Postion T-Bar to the center of of Change the mouse mode to Fis Change the mouse mode to His Change the mouse mode to His Change the mouse mode to His Park -Bar on the center of digs
Keyboard Map		Fig 3-103: Op	file. Hot key A B T E H Cod + A Odd + B	ic Analyzer H More waveform to where takes. More waveform to where takes Position 1-3ar to the center of of Change the mouse mode to The Change the mouse mode to The Dut A-Bar on the center of disp Put A-Bar on the center of disp
Keyboard Map		Fig 3-103: Op Place the A Bar position Place the A Bar position Place the T Bar position Place the T Bar position Change to Enclose mode Change to Enclose mode Change to Hand mode Plat A Bar Put B Bar Ele -> Graph	File.	ic Analyzer H More waveform to where takes. More waveform to where takes Postion T-Dar to the center of Change the mouse mode to A Pia A-Bar on the center of displ Put B-Bar on the center of displ Put B-Bar on the center of displ
Keyboard Map		Fig 3-103: Op Fig 3-103: Op Place the A Bar position Place the A Bar position Place the B Bar position Place the B Bar position Change to Enclose mode Change to Hend mode Plat A Bar Plat B Bar Ele -> Graph Data ->Enclose	file. Hot key A B T E H Carl+A Carl+B Carl+C Carl+E	ic Analyzer H More waveform to where takes. More waveform to where takes. Postion T-Bar to the center of the Change the mouse mode to En Change the mouse mode to Ha Park -Bar on the center of disp Put Bar on the center of disp Open the dialogue of Capture G To transfer the mode of mouse
Keyboard Map		Fig 3-103: Op	file.	ic Analyzer H More waveform to where takes. More waveform to where takes. More waveform to where takes Postoon T-Bar to the center of to Change the mouse mode to Fa Par ABar on the center of disp Par BBar on the center of disp Quen the dialogue of Capture G To transfer the mode of mouse Search speedic data with prede
Keyboard Map		Fig 3-103: Op Fig 3-103: Op Place the A Bar position Place the A Bar position Place the B Bar position Place the B Bar position Change to Enclose mode Change to Hend mode Plat A Bar Plat B Bar Ele -> Graph Data ->Enclose	file. Hot key A B T E H Carl+A Carl+B Carl+C Carl+E	ic Analyzer H More waveform to where takes. More waveform to where takes Postion T-Bar to the center of disp Postion T-Bar to the center of disp Park Bar on the center of disp



#### Fig 3-104: The Table of Keyboard Map



### Tip:

The function of Software Version Information Display for ZEROPLUS LA means that the software will open a small window which displays the software version, new functions and bug modifications when activating the software. It is convenient for users to know the information of the present software version.

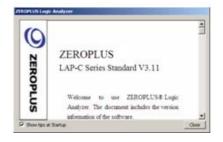


Fig3-107: Software Version Information Display Window



### Right Key

Menu Item

#### **Right Key Menu on the Bus/Signal Column**

#### Tip:

The Right Key menu is added on the basis of the Bus/Signal menu. So the function of Sampling Setup, Channels Setup, Bus Property, Group into Bus, Ungroup from Bus, Format Row and Rename are the same as those in the Bus/Signal menu. And the function of the Analog Waveform is the same as that in the Tools menu.

#### **Detail Menu & Dialog Box**



Fig 3-108: Right Key Menu on the Bus/Signal

Column

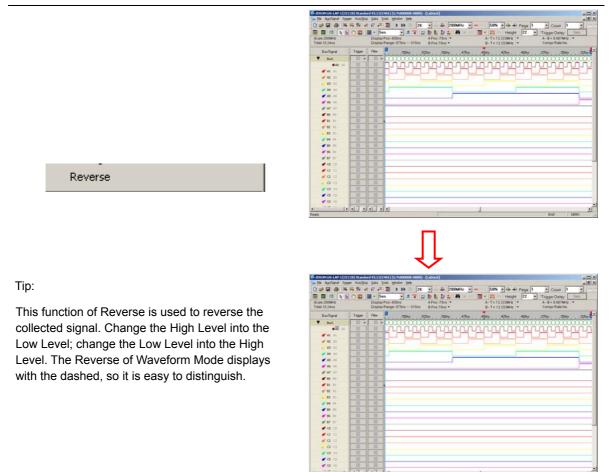


Fig3-109: Reverse Function Displayed in the Waveform Window



Add Channel	Add Channel       Image: Channel: A0         Channel: A0       Image: Channel: Channel: Channel: Channel: Channel         Image: Channel: Channel
	column.
Copy Channel	ZEROPLUS Logic Analyzer         Do you want to copy the channel ?         OK         Cancel         Fig 3-111: Copy the selected channel in Bus/Signal column.
Delete Channel	ZEROPLUS Logic Analyzer         Do you want to delete the channel ?         OK         Cancel         Fig3-112: Delete the selected channel in Bus/Signal column.
Delete All Channels	ZEROPLUS Logic Analyzer       X         Mail the Buses and channels will be deleted. Do you want to continue?         OK       Cancel         Fig 3-113: Delete all Buses and channels in Bus/Signal column.         ZEROPLUS Logic Analyzer         Mail the Buses and channels will restore to the default. Do you want to continue?         OK       Cancel
Restore Default Channels	Fig3-114: Restore the deleted Buses and channels in Bus/Signal Column.



### Tip:

The functions of the right key menu on the waveform area are similar to those of the Data menu.

The menu adds the functions, such as Place Ds and Dp, Add Bar in the waveform display area.

	Find Data Value Find Pulse Width Go To Place	Ctrl+F
<b>+</b> ≧ Ba⊨	Add Bar	
N	Zoom	E
87	Hand	н
R	Normal	ESCAPE
<b>333</b>	Show all Data	F10
ŝ	Previous Zoom	Ctrl+Z
	Data Format	)
	Waveform Mode	•
·	Color	
	Color Bus Data Color	

The Zeroplus Logic Analyzer

User's Manual V3.11

Fig3-115: Right Key Menu on the Waveform Area

	Place		Place A Bar
<b>+ </b> 2 Ba⊢	Add Bar		Place B Bar
<b>₿</b>	Zoom	E	Place Ds Bar
Ö	Hand	н	Place Dp Bar
R	Normal	ESCAPE	Place More

### Tip:

The right key menu on the waveform area adds the function of Place Ds and Place Dp. However the functions are only used after the Ds and Dp bars are activated, otherwise they will be disable. These functions are the same as that of A Bar.

When the mouse is stopped at a special position, click the right key on the mouse, select the Place Ds or Place Dp, the Ds or Dp bar will move to the special position.

For example, Open "Select an Analytic Range", select the special position is "-10", and then select "Place Ds". See the figure in the right column.

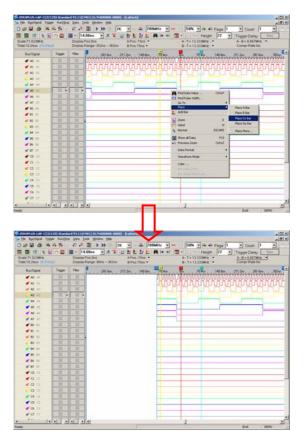


Fig3-116: Place Ds Bar

FM07I4A



He Add Bar

### Tip:

When the mouse is located at a special position on the waveform area, click the right key to select the Add Bar function; a bar will be added automatically in the special position according to the sequence of the word and color. See the C Bar in the position "5" in the right column.

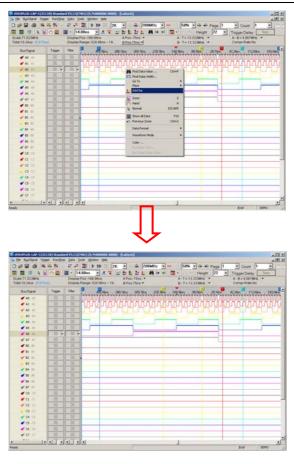


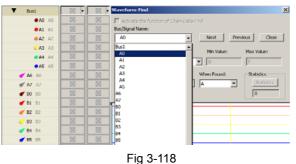
Fig3-117: Add a Bar on the Waveform Area.



# 3.2 Find Data Value

Find Data Value is a very useful tool to help the user to find data on the received signals.

- Step1. Click the find data value 🗰 icon; the dialog box of Waveform-Find will appear.
- Step2. Using the pull-down menu, select the Bus/Signal Name.
  - The Bus/Signals listed on the pull-down menu represent the status of the Bus/Signal column as shown in Fig 3-118.



Step3. Choose the character for Find. The list of characters depends on whether it is a Bus, Signal, or the protocol analyzer such as I2C, UART, SPI, etc., which is being searched (See Figs 3-119, 3-120, 3-121, 3-122, 3-123, 3-124, 3-125, 3-126 and 3-127).

Bus: Choose among = , != , In Range and Not In Range (Enter the Min Value or Max Value).

**Protocol Analyzer:** Choose the segments bits of the protocol analyzer (Select the protocol analyzer item and enter the value for Min Value or Max Value).

Signal: Choose among Rising Edge, Falling Edge, Either Edge, High or Low.

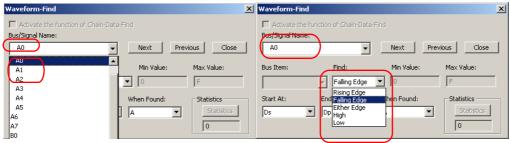


Fig 3-119: Waveform-Find Dialog Box of the Logic Signal

Waveform-Find	×	Waveform-Find	×
Activate the function of Chain-Da Bus/Signal Name: Bus2 Bus1	ta-Find           Next         Previous         Close	Activate the function of Chain-Data-Find Bus2 Next Previous Close	
A0 A1 A2 A3 A4 A5	Min Value: Max Value: Value: Max Value: Value: Max Value: Value: Statistics Value: Statistics Statistics	Bus Item:     Find:     Min Value:     Max Value:       Data     I=     00     F       Start At:     Endition     F     Statistics       Ds     Dp     In Range     Statistics	- -
A6 Bus2	0	0	

Fig 3-120: Waveform-Find Dialog Box of the Logic Bus

Waveform-Find		Þ	Waveform-Find			×
Activate the function of Chain-Data Bus/Signal Name:	a-Find		Activate the function Bus/Signal Name:	on of Chain-Data-Fir	ıd	
Bus1	Next Pr	evious Close	Bus1	-	Next Pre-	vious Close
A0	Min Value:	Max Value:	Bus Item:	Find:	Min Value:	Max Value:
A1 A2		F	Start 🔹			F
A3 A4 A5	When Found:	Statistics Statistics	ADDRESS		When Found:	Statistics Statistics
A6 A7		0	Write A-ACK			0

Fig 3-121: Waveform-Find Dialog Box of the Protocol Analyzer I2C



Waveform-Find		x	Waveform-Find	×
Activate the function of Chain-Data	a-Find		Activate the function of Chain-Data-Find	
Bus/Signa Name:			Bus/Signal Name:	
A1	Next Previous Close		A1 Next Previous Close	1
Bus1 A0	Min Value: Max Value:		Bus Item: Find: Min Value: Max Value:	
	▼ 0 F	1	A-ACK Faling Edge 0 F	
A3	When Found: Statistics		Start At: End Falling Edge hen Found: Statistics	ור
A4 A5	A Statistics		Ds Dp High	
A6	0			



Waveform-Find	X Waveform-Find
C Activate the function of Chain-Data-Find	Activate the function of Chain-Data-Find
Bus/Signal Name:	Bus/Signal Name:
Bus2   Next Previous Close	Bus2   Next Previous Close
Bus1 Min Value: Max Value:	Bus Item: Find: Min Value: Max Value:
A2 A3 When Found: Statistics	Start dAt: When Found: Statistics
A4	Data P A Statistics
A5 0	Odd Party 0
A6	

Fig 3-123: Waveform-Find Dialog Box of the Protocol Analyzer UART

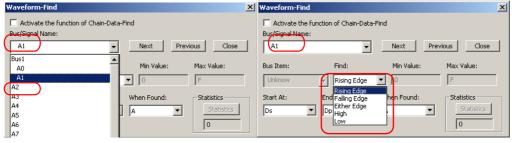
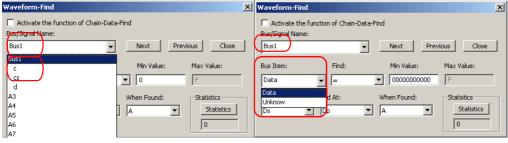


Fig 3-124: Waveform-Find Dialog Box of the UART Signal





Waveform-Find	X Waveform-Find	×
Activate the function of Chain-Data-Find	Activate the function of Chain-Data-Find	
B <del>us/Signal N</del> ame:	Bus/Signal Name:	
cs   Next  Previous  Close	cs Vext Previous Close	
Busi		
Min Value: Max Value:	Bus Item: Find: Min Value: Max Value:	
CS 0000000000 F	Data 🖌 Falling Edge 💌 00000000000000000000000000000000000	
d	Rising Edge	
A3 When Found: Statistics	Start At: End Faling Edge hen Found: Statistics	1
A4 Statistics	Ds Dp Either Edge Statistics	
A5		
A6 0		
A7		1

Fig 3-126: Waveform-Find Dialog Box of the SPI Signal



Waveform-Find	Waveform-Find
C Activate the function of Chain-Data-Find	C Activate the function of Chain-Data-Find
Bus/Signal Name:	Bus/Signal Name:
SPI Next Previous Close	SPI Vext Previous Close
Bus Item: Find: Min Value: Max Value: Data	Bus Item: Data In Range Start At: Ds Dp Not In Range Min Value: Min Value: Min Value: Min Value: Min Value: Min Value: Min Value: Min Value: Min Value: Min Value: Statistics Statistics 0 0 0 0 0 0 0 0 0 0 0 0 0

Fig 3-127: Waveform-Find Dialog Box of the Bus Item of the SPI Signal

Step4. Choose the position to start the search by selecting one of the following: Start At: Ds T , A, B, C, etc.; End At: Dp, A, B, C, etc.. Then click Next or Previous to search it.

When Found: Choose a Bar to mark the result: A, B, C, etc..

- Step5. Click Statistics to show the number of instances of the search results.
- Note: It is available only when searching through a Bus.

cale:3.04128ns otal:20.48us			Pos:=10.15us A Pos:=10.15us ▼ A = T = 10.15us ▼ Range:=10.226032us B Pos:150ns ▼ B_T T = 150ns ▼
Bus/Signal	Trigger	Filter	-10. 210826uz-10. 195619uz-10. 180413uz-10. 165206us 10. 1545 -10. 134794uz-10. 11
Bus1	-		(0x01)(0x02)(0x03)(0x04)(0x05)(0x06)(0x07)(0x08)(0x09)(0x0A)(0
• A0 A0			10ns 10ns 10ns 10ns 10ns 10ns 10ns 10ns
●A1 A1			Tavefors-Find
<b>A2</b> A2			Activate the function of Chain-Data-Find
<mark>⊂ A3</mark> A3			Bus/signai Name:
<b>0 A4</b> A4			Bus1   Previous Close
🥑 A5 A5			Bus Item: Hin Value; Max Value:
🥑 A6 A6			Data 💌 = 💌 8 FF
<b># A7</b> A7			Start At: End At:
<b>60</b> B0			Ds Dp A Statistics
<b>d B1</b> B1			Address: -1015
<b>♂ B2</b> B2			

Fig 3-128: The A Bar is placed at the 0X08 of Bus1 where the condition of the Waveform-Find is set. The Statistic of Waveform-Find shows a "64".

Scale:2.3576ns Total:20.48us			Pos:-9.97us         A         T         =         9.97us         ▼           Range:-10.02894us         ~          B         Pos:150ns         ▼         B         -T         =         150ns         ▼
Bus/Signal	Trigger	Filter	-10.017152u=10.005364u=-9.993576us -9.981788us -5.974s -9.958212us -9.946424u
Bus1	-	•	0X14 (0X15 (0X16 (0X17 (0X18 (0X1 <mark>9 (0X</mark> 1A (0X1B (0X1C )
			10ns 10ns 10ns 10ns 10ns 10ns 10ns 10ns
●A1 A1			20 Taveform-Find 20
<b>A2</b> A2			Activate the function of Chain-Data-Find
<mark>⊂</mark> <b>A</b> 3 A3			Buc/Signal Name:
<b>0 A4</b> A4			Bus1
🧹 A5 A5			Bus Item: Find: Min Value: Max Value:
🥑 A6 A6			Data = 1 IA FF
<b>« A7</b> A7			Start At: End At: When Found: Statistics
<b>e BO</b> BO			Ds Dp A Statistics
🥑 B1 B1			Address: -997
🥑 <b>B2</b> B2			
	8	×***×	

Fig 3-129: The A Bar is placed at the 0X1A of Bus1 where the condition of the Waveform-Find is set.



Scale:5.6539625 Total:32768		Display Pos:0         A Pos:104         ▼         A - T = 104         ▼           Display Range:-141 ~ 143         B Pos:0         ▼         B - T = 1         ▼
Bus/Signal	Trigger	Filter -113.079-84.809 -56.54 -28.27 28.27 56.54 84.809 113.
Bus (SPI)	•	
●AO AO	х	
●A1 A1	X	
<b>e A2</b> A2		
<mark>. A3</mark> A3	X	Tavefors-Find
<b>0 A4</b> A4		Activate the function of Chain-Data-Find      Best/Signal Name:
🥑 A5 A5		Bust         V         Next         Previous         Close
🥑 A6 A6		Eus Item: Find: Min Value: Max Value:
✓ A7 A7		
🥑 BO BO		Start At: End At: When Found: Statistics
🥑 B1 B1		Address: 0
🥑 B2 B2		
🥑 B3 B3		
🥑 B4 B4		

Fig 3-130: The B Bar is placed at the 0X12 of Data of Protocol Analyzer SPI where the condition of the Waveform-Find is set.



## **3.3 Statistics Feature**

Section 3.3 presents detailed information on the **Statistics** feature in the software interface. The **Statistics** feature presents user information pertaining to nine periodicities: **Full Period**, **Positive Period**, **Negative Period**, **Conditional Full Period**, **Conditional Positive Period**, **Conditional Negative Period**, **Start Pos**, **End Pos** and **Selected Data**.

Click on the Statistics icon 🛗, and an interface like Fig 3-131 or Fig 3-132 will appear.

* C	Channel Selection Column Selection Condition Parameter Warning Parameter Refresh 🗖 Statistics Filter										
	HANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selected Data	
A	0	211	212	211	0	0	0	Ds	Dp		
A	1	52	53	52	0	0	0	Ds	Dp		
A:	2	0	0	1	0	0	0	Ds	Dp		
A	3	0	0	1	0	0	0	Ds	Dp		
A	4	0	0	1	0	0	0	Ds	Dp		
A!	5	0	0	1	0	0	0	Ds	Dp		
A	6	0	0	1	0	0	0	Ds	Dp		
A	7	0	0	1	0	0	0	Ds	Dp		
B	)	0	0	1	0	0	0	Ds	Dp		
B:	1	0	0	1	0	0	0	Ds	Dp		<b>•</b>

	i-LAP-C(321 Signal Trigg				:000000-0000) - [	12C]						-	- 10
					▶ □ 2K		ELU	5	0V - A	6. Dune 1	-		
											Count		4
		0					<b>₩</b> 网 1+		📅 🍖 🛛 Heig		Trigger Delay		ц
cale:689.5 stal:78.60				Pos:145.0 Range:10	21634us 8.766225us ~	A Pos:-52.0 B Pos:-52.0			F = 19.198Hz T = 19.2Hz   ▼		A - B = 166.66 Compr-Rate:1		
Bus/S	ignal	Trigger	Filter	<b>.</b>	16.017307up 123.26	8389up 130.5	1947us, 137.77	1552ug 145.02163	Hun 152.272716	uq 159.523797uq 166	.774879up 174.0	2596/up181.27	m
🔻 Bu	st (I2C)		0	0001	D-AQ	DATA : 0	K23	D-AO	D	ATA : 00(45	D-AQ	DATA: 0X67	
	04 0A0	x				0.0	0.0.0				0 0 0	חחו	
	• A1 A1												ī
	A2 42		0	ir -									ľ
	A3 A3		0.										
🗸 A4			8										
	A5		8										-
🝼 A6			$\otimes$										_
💣 A7	A7												
🍼 B0	80												
🥑 B1	B1		8										
🥑 B2	82		8	1									
🥑 B3	83		8	1									
🕑 D4	D4			1									
<b>d</b> 85	15	10	8										
		रा है म	स ी ज							1			7
hannel Se		and and	and the second second	d tank i	Warning Parameter	Refresh	☐ Statistics	filter		-			
HANNEL	Full Peri	od Posi	tive Per	Negative P	Conditional	Conditional .	Conditional	Start Pos	End Pos	Selected Data			
40 41	211 52	212		211 52	0	0	0	D5	Dp				
2	0	53		1	0	0	0	Ds Ds	Dp				
3	0	0		1	0	0	0	Ds .	Dp				
16	0	0		1	0	0	0	Ds	Dp				
6 6	0	0		1	0	0	0	Ds Ds	Dp Dp				
17	0	0		î.	0	0	0	Ds Ds	Dp				
0	0	0		1	0	0	0	Ds	Dp				
1	0	0		1	0	0	0	Ds .	Dp				

Fig 3-131: Statistics table

Fig 3-132: Logic Analyzer with Statistics Enabled

There are four options for adjusting how statistical information may be presented. These four options are **Channel** Selection, Column Selection, Condition Parameter and Warning Parameter.

### **Channel Selection**

Channel S	elec	tion							x
	7	6	5	4	з	2	1	0	
Port A	◄	◄	$\overline{\mathbf{v}}$	◄	◄	◄	◄	$\overline{\mathbf{v}}$	
Port B	•	◄	◄	◄	$\overline{\mathbf{v}}$	◄	$\overline{}$	◄	
Port ⊂	◄	◄	$\overline{\mathbf{v}}$	◄	◄	◄	◄	$\overline{\mathbf{v}}$	
Port D	Г							Г	
Port E	Г			Г					
Port F	Г		Г				Г	Г	
Port G	Г								
Port H	Г		Г					Г	
Port I	Г	Г	Г	Г	Г		Г	Г	
Port J	Г	Γ		Γ	Γ	Γ	Γ	Γ	
Port K	Г					Г			
Port L	Г							Г	
Port M	Г		Γ				Γ	Γ	
Port N	Г					Г			
Port O	Г					Г			
Port P	Γ		Γ						
Select	all	Cle	ar all		OK		Ca	ncel	

Fig 3-133: **Channel Selection**. Allow the choice of pins in which port will be included in the statistical analysis of a test run.



<b>Column Selection</b>	n
-------------------------	---

Column Selection	×						
Probe							
🔽 Full Period							
Positive Period	Positive Period						
🔽 Negative Period							
🔽 Conditional Full Period							
🔽 Conditional Positive Period							
🔽 Conditional Negative Period							
🔽 Start Pos							
🔽 End Pos							
🔽 Selected Data							
OK Cancel							

Fig 3-134: **Column Selection**. Allow the choice of items which will be considered in the statistical results.

Condition Parameter		
	Condition Parameter	×
	Conditional Full Period	
	400ns <= Time <= 400ns	
	Conditional Positive Period	
	200ns <= Time <= 200ns	
	Conditional Negative Period	
	200ns <= Time <= 200ns	
	OK Cancel	

Fig 3-135: **Condition Parameter.** Allow the setting of time intervals for Conditional Full Period, Conditional Positive Period and Conditional Negative Period.

Channel Selection Column Selection Condition Parameter Warning Parameter Refresh Statistics Filter										
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selected Data	
A0	211	212	211	0	0	0	Ds	Dp		
A1	52	53	52	0	0	0	Ds	Dp		
A2	0	0	1	0	0	0	Ds	Dp		
A3	0	0	1	0	0	0	Ds	Dp		
A4	0	0	1	0	0	0	Ds	Dp		
A5	0	0	1	0	0	0	Ds	Dp		
A6	0	0	1	0	0	0	Ds	Dp		
A7	0	0	1	0	0	0	Ds	Dp		
B0	0	0	1	0	0	0	Ds	Dp		
B1	0	0	1	0	0	0	Ds	Dp		•

Fig 3-136: The Numbers of Data Qualified by Condition Parameter



### Warning Parameter

Warning Paramel			×
Conditions	Min	Max	
Period	🔽 10us	✓ 100us	
C Frequency	☐ 10KHz	100KHz	
	ОК	Cance	

Fig 3-137: Warning Parameter. Set the conditions which will be marked to call users' attention.

Channel Sele	Channel Selection Column Selection Condition Parameter Warning Parameter Refresh 🔽 Statistics Filter									
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selected Data	<u> </u>
A0	211	212	211	0	0	0	Ds	Dp		
A1	52	53	52	0	0	0	Ds	Dp		
A2	0	0	1	0	0	0	Ds	Dp		
A3	0	0	1	0	0	0	Ds	Dp		
A4	0	0	1	0	0	0	Ds	Dp		
A5	0	0	1	0	0	0	Ds	Dp		
A6	0	0	1	0	0	0	Ds	Dp		
A7	0	0	1	0	0	0	Ds	Dp		
B0	0	0	1	0	0	0	Ds	Dp		
B1	0	0	1	0	0	0	Ds	Dp		

Fig 3-138: The numbers of data qualified by warning conditions are printed in black, otherwise in red.



# 3.4 Customize Interface

Section 3.4 presents detailed instructions pertaining to how to **modify** the **Waveform Display Mode**, how to **modify** the **Ruler Mode**, how to **modify** the **Waveform Height**, and how to **modify** the **Correlated Setting**.

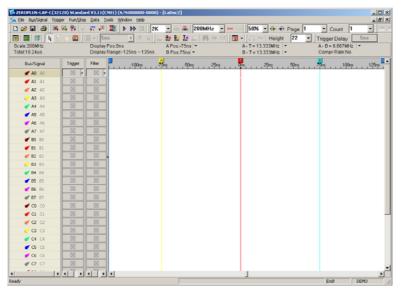


Fig 3-139: The Interface Layout Shown in Default Settings

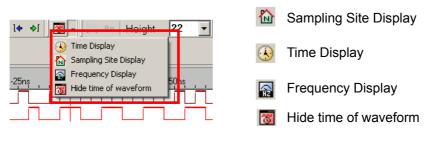


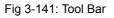
## 3.4.1 Modify Waveform Display Mode

To modify the display mode, users can use icons on the tool bar/box, or menu. For the menu, go to **Tools** and click **Customize**. See *Fig.3-14*0

📹 Customize	Customize
Tolor Setting	Common Setup Toolbars Shortcut Key Auto Save
Bus Property         Refresh Protocol Analyzer         Multi-stacked Logic Analyzer Settings         Analog Waveform         DSO-stacked Settings	Vaveform Display Mode         Sampling Site Display       Frequency Display         Time Display       Hide time of waveform         Regular Ruler       Waveform Setting         Regular Ruler       Font Size         Time/Sampling Site Ruler       Font Size         Correlated Setting       Open/Close Compression Warning         Show Gridine       Show the T Bar in the middle area         Show Toolhip       Open/Close Double Warning         When the roller is moved toward back, the Time Axis in the waveform area will move toward light.         Data Process         What do you want to show when you press the Stop during the running?         Keep the Present Data       Read the Captured Data         OK       Cancel       Help

Fig 3-140: Customize the Display Mode by Using the Tool Bar





**Waveform Display Mode** – There are four display modes to determine the method of capturing data from sampling: Sampling Site Display, Time Display, Frequency Display and Hide time of waveform.



## 3.4.2 Modify Ruler Mode

Use the menu to modify the Ruler Mode.

Go to Tools and click Customize. See Fig. 3-142

istomize 🛛 🔀								
Common Setup Toolbars Shortcut Key Auto Save								
Waveform Display Mode								
C Sampling Site Display	C Frequency Display							
C Time Display	Hide time of waveform							
- Ruler Mode	Waveform Setting							
C Regular Ruler	Waveform Height 22 💌							
Time/Sampling Site Ruler	Font Size 12 💌							
	Common Setup Toolbars Shorter Waveform Display Mode Sampling Site Display Time Display Ruler Mode Regular Ruler							

Fig 3-142: Ruler Mode

### **Regular Ruler**



Fig 3-143: Scales in Regular Ruler

### Time/Sampling Site Ruler



Fig 3-144: Scales in Time/Sampling Site Ruler

**Ruler Mode** – There are two styles of Ruler: (Regular Ruler, Time/Sampling Site Ruler) **Regular Ruler:** 

Presented in increments of 5.

Time/Sampling Site Ruler (default):

Presented in increments of 25ns.



## 3.4.3 Modify Waveform Height & Correlated Setting

To modify Waveform Height, click **Tools → Customize**.

### **Waveform Height**

Set the height of waveform (18-100) in chosen items at toolbar that will show the amplitude of the waveform.

Customize	×
Common Setup Toolbars Shortcut	Key Auto Save
Waveform Display Mode	
C Sampling Site Display	Frequency Display
C Time Display	Hide time of waveform
- Ruler Mode	Waveform Setting
C Regular Ruler	Waveform Height 22 💌
• Time/Sampling Site Ruler	Font Size 12

Fig 3-145: Waveform Height

Waveform Height = 40

### Waveform Height = 18

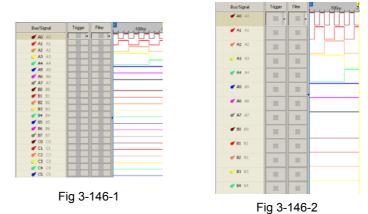


Fig 3-146: Examples of Waveform Height

### **Correlated Setting**

Select **Auto-Close** in the following figure.

Correlated Setting	🔲 Open/Close Compr	ession Warning							
🔲 Show Gridline	🔽 Show the T Bar in t	he middle area							
🔽 Show Tooltip	🔽 Open/Close Double	e Warning							
When the roller is m waveform area will r	oved toward back, the T move toward right.	lime Axis in the							
Data Process What do you want to show when you press the Stop during the running?									
Keep the Present Data									
Check for Update <u>R</u> estore Defaults									
	ОК С	Cancel Help							

Fig 3-147: Correlated Setting

Bus/Signal	Trigger	Filter	-25ns -
🥑 AO AO	•	•	
🥑 A1 A1			
🥑 A2 A2			
🧹 A3 A3			
🥑 A4 A4			
🧹 A5 A5			
🥑 A6 A6			
🝼 A7 A7			
🥑 BO BO			
🥑 B1 B1			

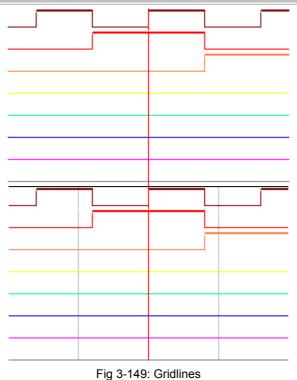
Bus/Signal	Trigger	Filter	25ns -18,75n:
🥑 AO AO	•	•	
🝼 A1 A1			
🥑 A2 A2			
🧹 A3 A3			
🥑 A4 A4			
🥑 A5 A5			
🥑 A6 A6			
✓ A7 A7			
🥑 BO BO			
🥑 B1 B1			

Fig 3-148: An Example for Auto-Close

**Auto-Close** - With the cursor in the channel, when users try to drag a Bar, the Bar will stop at the approaching edge of the channel (Rising Edge or Falling Edge).

Tip: In the above example, when dragging the C Bar, the A Bar will stop at the Raising Edge of A1.





Show Gridline - The gridlines will be displayed on the waveform area.

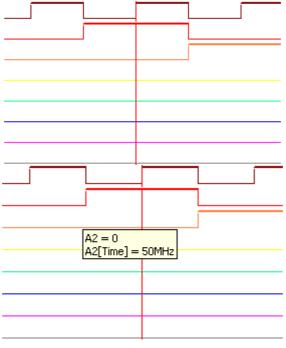


Fig 3-150 - Tooltips

Show Tooltip - Leave the mouse over a waveform and the description will be shown.

Show the T Bar in the middle area -Show the T Bar in the middle of the Waveform Display Area after triggering.

### When the roller is moved toward back, the Time Axis in the waveform area will move toward right-

When the option is selected and users move the roller in the middle of Mouse directly toward back, the scrollbar will move toward right correspondly.

Check for Update:The Logic Analyzer software will automatically check for updates when being started.Restore Defaults:The Waveform Display Mode, Ruler Mode, Waveform Setting, Correlated Setting and Data<br/>Process will return to the default setting.



## 3.5 Auto Save

To save the captured data for a long time, users can use icons on the tool bar/box, or menu.

For the dialog box, go to **File** menu to click **Auto Save** or go to **Tools** menu to select **Customize** and select **Auto Save**. See *Fig 3-151*.

Ctrl+N
Ctrl+0
Ctrl+F4
Ctrl+S
Ctrl+Shift+E
Ctrl+C
۲
Ctrl+P

Customize	×
Common Setup   Toolbars   Shortcut Key   Auto Save	
⊽ <u>Activate</u> File Name: ∐A	
Save Path C:\Documents and Settings\Administrator\My	
C: Mocuments and Settings'Administrator/My Repetitive Run Time Interval: Data Display Menu Renewal Mode © Every Renewal © Open the first file after Stopping the Run Default	
OK Cancel Help	

Fig 3-151-1: Auto Save on File Menu

Fig 3-151-2: Auto Save Item of Customize

Fig 3-151: Auto Save

Auto Save: The default is not activated; after activating, it keeps working and users also can choose Cancel to close it.

Activate: The default is not activated: after activating, it keeps active and users also can choose **Cancel** to close it. **File Name**: Before users name the file, the file name is defaulted as LA. In fact, the saved file name can add a serial number for the file automatically.

Save Path Name: Users can enter the path directly or choose the path from the selected path button

**Time Interval**: When the auto save function is activated, the time interval from one finished sampling to the next activated sampling can be set according to users' requirements; the default is 1s, and the unit can be selected from s(second), m(minute) and hr(hour).

**Every Renewal**: When the repetitive run is activated, the waveform image or the state image will renew again and again.

**Open the first file after stopping the Run**: When the repetitive run function is activated, the waveform only displays the first file and it isn't renewed; when the repetitive run is stopped, the waveform still displays the first file.



Fig3-152: Auto Save



# 3.6 Color Setting

To modify Color, click **Tools → Color Setting** 

/orkaround Waveform			
Name	🗌 🗖 Relating	Color	<b>▲</b>
Waveform Background List Background 1 List Background 2			
Cursor Grid			
Unknown Line Default Bus			
Bus Text List Text			
Time Text Bus Error			
Bus Error Text Signal Filter Bar			-
<u> </u> •			
O         1         O           10         10         10         10	0 0 0	1 altered, co	ackground is rrresponding color ally changes to the contrast
		When beit background	ng printed, the nd is white.

Fig 3-153: Workaround and Waveform Color Setting

Workaround - Set the workaround color of the Logic Analyzer and the text.

orkaround Waveform			
Name	🗖 Relating	Color	-
Waveform Background			
List Background 1			
List Background 2			
Cursor			
Grid			
Unknown Line			
Default Bus			
Bus Text			
List Text			
Time Text			
Bus Error			
Bus Error Text			

Fig 3-154: Workaround Color Interface

Waveform Background: The Logic Analyzer's Waveform Viewer Background Color.

List Background 1: The Logic Analyzer's First Listing Viewer Background Color.

List Background 2: The Logic Analyzer's Second Listing Viewer Background Color.

All optional items include the current color of Cursors, Grid, Unknown Line, Default Bus, Bus Text, List Text and Time Text (users can scroll the vertical wheel to view the selectable items).

Bus Error: Users can configure the color of Bus Error Data from the Color Setting dialog box.

Bus Error Text: Users can configure the color of Bus Error Text from the Color Setting dialog box.

Signal Filter Bar: Users can configure the color of Signal Filter Bar from the Color Setting dialog box.

Relating: When users select one item to change the color of the item, and users want to change other items into

the same color, they can select other items at the same time in the Relating column, then the selected items will

be changed into the same color. So it is convenient for users to change many items into the same color once.

After the background is altered, corresponding color automatically changes according to the contrast ratio: When users set the color for the workaround and select the option, the system will switch other colors automatically to become the contrast color.



When being printed, the background is white: When being printed, the background color is white.

Name	🗌 🔲 Relating 📗	Color	Linewidth
A0			1 pixel
A1			1 pixel
A2			1 pixel
A3			1 pixel
Α4			1 pixel
A5			1 pixel –
A6			1 pixel
A7			1 pixel
BO			1 pixel
B1			1 pixel
B2			1 pixel
B3			1 pixel
B4			1 pixel
B5			1 pixel
R6			I 1 nivel I
Preview			
	10		

Waveform - Change the color of the Buses or signals on the waveform area.

Fig 3-155: Waveform Color Interface

Waveform: The channel color can be varied by users.

Linewidth: The linewidth can be adjusted by the users' requirements; there are three options which are 1pixel, 2 pixel and 3 pixel.



# 3.6.1 Modify Workaround Color

To modify the workaround color, click the color block shown in Fig 3-154. A **Color** panel, shown in Fig 3-156, will appear. Select a color shown on the panel or click on **Define Custom Colors** to create the desired color.

Color	<u>? ×</u>
<u>B</u> asic colors:	
с., ,	
	Hug: 160 <u>R</u> ed: 0
	<u>S</u> at: 0 <u>G</u> reen: 0
Define Custom Colors >>	ColorIS <u>o</u> lid Lum: 0 Blue: 0
OK Cancel	Add to Custom Colors

Fig 3-156: Color Panel with Its Advanced View



## 3.6.2 Modify Waveform Color

Foreground color refers to the color of the output signal lines in the Waveform Display Area. *Fig3-157* presents how to change colors of a signal or some signals. Repeat the following procedures if users need to change colors of many signals.

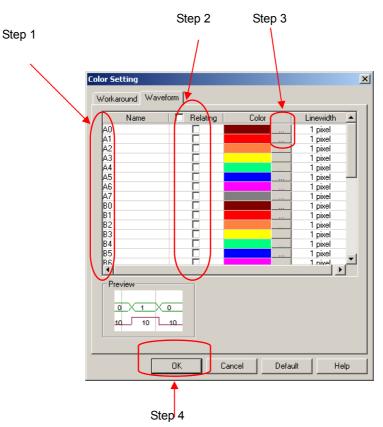


Fig 3-157: Stepwise Illustration of Changing Waveform Colors

- Step 1: Select several Optional Items.
- Step 2: Select the corresponding items in the relating.
- Step 3: Choose a color by following the method shown in Fig 3-157.

Step 4: Click **OK** to change their colors into the same, for example A1, A2, A3 and A4.

Here is a sample of an altered Logic Analyzer software interface which will be used for further demonstrations in subsequent chapters. See *Fig 3-158.* 

		- 5n	and a state of the	2K		. 200	MH2 *		58%			Count     Trigger Delay	561
cale 200MHz otal 10.24us		Display P Display P	lange-125na -	135ns	APps-7 BPos7				A-T=133 B-T=133			A - B = 6.867M Compr-Rate N	
Bus/Signal	Trigger	Film	-100	÷	-	50m .				m .	50m		125
# AQ 40	201	100											
# AL AL	26	30											
💓 AZ AZ	25		1		5		_		1				1
- A3 43	25												
# A4	26			-			_						
# A5 A5	10											-	
# A6 40	28												
# A7 32	121												
<b>#</b> 80 mil	N												
🕑 BL 11	12												
🛷 82 III	1.95	- 10											
6 83 11	24												
<b>6</b> 84 84	M.							_					
💣 85 m	20												
# DL 11	26												
af \$7 U	- 24	- 36 -						_					
e co ca	21	28		_				_				_	
🖌 🛛 🖓	M							_				_	
e a a	M							_					
e a o	24												
🕊 CK 01	25							_					
2 CS CS	25							_				_	
# 05 CK	12							_					
100	30												

Fig 3-158: An Altered Interface Sample to Be Used in Subsequent Chapters



# 3.7 The Flow of Software Operation

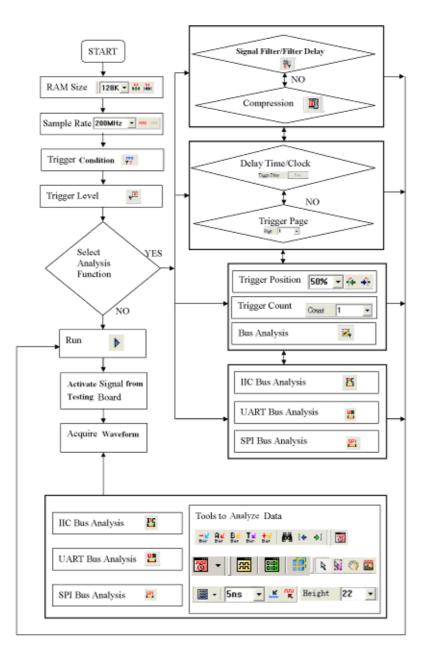


Fig 3-159: Software Flow Diagram

# Conclusion

Information demonstrated in this chapter is only for entrance level. There are more advanced approaches which may require fewer steps than those shown in this chapter. This chapter is meant to equip users with sufficient grounding of the Logic Analyzer's software interface.



# **4 Introduction to Logic Analysis**

- 4.1 Logic Analysis
- 4.2 Bus Logic Analysis
- 4.3 Plug Analysis
- 4.4 Bus Packet List
- 4.5 Bus Analysis
- 4.6 Compression
- 4.7 Signal Filter and Filter Delay
- 4.8 Noise Filter
- 4.9 Data Contrast
- 4.10 Refresh Protocol Analyzer
- 4.11 Memory Analyzer
- 4.12 Multi-stacked Logic Analyzer Settings
- 4.13 DSO-stacked Settings



# Objective

Chapter 4 gives detailed instructions on performing two basic analysis operations and other advanced analysis applications with the Logic Analyzer. These two basic analysis operations are the Logic Analysis and the Bus Logic Analysis, which are fundamental to all further applications. The other advanced analysis applications are the I2C (Inter Integrated Circuit) Analysis and the UART (Universal Asynchronous Receiver Transmitter) Analysis, the SPI (Synchronous Peripheral Interface) Analysis, Compression, Signal Filter Setup, and Filter Delay Setup, etc..

## 4.1 Logic Analysis

Logic Analysis is meant for a single signal analysis. Section 4.1 gives detailed instructions on the software's basic setup.

Basic Software Setup of the Logic Analysis

### Task 1. Clock Source (Frequency) and RAM Size Setup

Step1. Click icon or click Sampling Setup from Bus/Signal on the menu bar, the dialog box as shown in Fig 4-1 will appear.

<u>.</u>	Sampling Setup	Sampling Setup	X				
	Channels Setup Signal Filter Setup	Clock Source     Asynchronous Clock     finternal Clock     Frequency: 200MHz					
	Group into BusCtrl+GUngroup from BusCtrl+U	Synchronous Clock					
	Expand Collapse	C Rising Edge Frequency: 1000Hz     C Faling Edge (Min:0.001Hz, Max:100MHz)     Note: The external clock voltage level is the same as the port A trigger level					
	Format Row Format Row	Sampling RAM Size RAM Size Compression Mode Signal Filter Signal Filter Setup Signal Filter Setup	J				
		Apply OK Cancel Restore Defaults Help					

Fig 4-1 - Clock Source

Step 2. Clock Source (Frequency) Setup

Internal Clock (Asynchronous Clock)

Click on **Internal Clock**, and then select the Frequency from the pull-down menu to set up the frequency of the device under test (DUT). The frequency of the Internal Clock must be at least four times higher than the frequency of the Oscillator on the DUT. Or, select the frequency from the pull-down menu on Tool Bar as Fig 4-2 shows.

**Tip:** Connect the output pin of the oscillator from the tested board to the signal connector of the Logic Analyzer to measure it by using the internal clock of the Logic Analyzer.

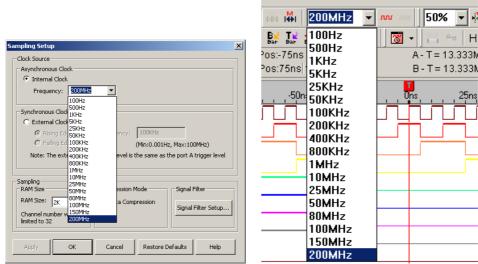


Fig 4-2 - Clock Source Pull-down Menu

External Clock (Synchronous Clock)

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

Click on **External Clock**, and then select "Rising Edge" or "Falling Edge" as the trigger condition of the DUT. In the Frequency column, type the frequency of the oscillator on the DUT.

**Tip:** The External Clock is applied when the frequency of the oscillator on the tested board is exceeds the range of the internal clock of the Logic Analyzer. Connect the output pin of the oscillator on the tested board to the CLK pin of the Logic Analyzer.

Step 3. RAM Size Setup

Click the RAM Size received or from the pull-down menu in the Sampling Setup dialog box as shown in Fig 4-3.

	128K 🔻	M M  441  4  4	-Sampling RAM Size		© Exter © R © F Note:	You have selected the Double Mode.Port C, Port D, the functions of Compression, Signal Filter Delay and Signal Filter Display Bar are not available under this	z)
ĸ	2K 16K 32K	B¥ T¥ Bar Ios:-75ns	Channel nur <sup>2k</sup> limited to 32	o∧	Sampling	Don't show me this warning again.	ger level
51	64K 128K 256K	os:75ns , ,-50r	64			umber will be	nal Filter Setup

Fig 4-3 – RAM Size

Tips 1: The Double Mode is available for the Modules in Table 4-1 except for the LAP-C(16032),

LAP-C(16064) Modules.

**2:** The relationship between RAM Size, Signal Filter Mode, Compression Mode and Channels as shown in Table 4-1 and Fig 4-3.

Status		Normal M	ode		Double I	Vode
Model No.	RAM Size/ Channels	Channels Available	Compression Mode & Signal Filter Mode	RAM Size/ Channel s	Channels Available	Compression Mode & Signal Filter Mode
LAP-16032U	2K ~ 32K	16 channels	Available	64K	16 channels	Disable
LAP-16064U	2K ~ 64K	16 channels	Available	128K	16 channels	Disable
LAP-16128U	2K ~ 128K	16 channels	Available	256K	16 channels	Disable



LAP-32128U-A	2K ~ 128K	32 channels	Available	256K	16 channels	Disable
LAP-321000U-A	2K ~ 1M	32 channels	Available	2M	16 channels	Disable
LAP-322000U-A	2K ~ 2M	32 channels	Available	4M	16 channels	Disable
LAP-C (16032)	2K ~ 32K	16 channels	Available	-	-	-
LAP-C (16064)	2K ~ 64K	16 channels	Available	-	-	-
LAP-C (16128)	2K ~ 128K	16 channels	Available	256K	16 channels	Disable
LAP-C (162000)	2K ~ 2M	16 channels	Available	4M	16 channels	Disable
LAP-C (32128)	2K ~ 128K	32 channels	Available	256K	16 channels	Disable
LAP-C (321000)	2K ~ 1M	32 channels	Available	2M	16 channels	Disable
LAP-C (322000)	2K ~ 2M	32 channels	Available	4M	16 channels	Disable

### Task 2. Trigger Property

-		Trigger Property	×
Ϋ́́́́́́́	Bus Trigger Setup	Trigger Content Trigger Delay Trigger Range	
ллг Т Т	Channel Trigger Setup		
, 🕄	Trigger Property	Port A	
İ.	Trigger Mark	[CMOS(5V) ▼ 2.5 (Y)	
÷.	Pulse Width Trigger Module(Option)	Port B (Min:1, Max:65535)	
1 1		TTL 1.5 M	
$\boxtimes$	Don't Care	Port C	
	High	TTL 1.5 (V)	
		Port D	
	Low	TTL 1.5 (M)	
Z	Rising Edge		
59	Falling Edge		
Xđ	Either Edge		
1000			
	Reset	OK Cancel Default Help	

Fig 4-4 - Trigger Property

### Step2. Trigger Level Setup

Click the pull-down menu of **Trigger Level** on Port A, B, C and D to select the Trigger Level as the voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep.

**Tip:** There are four commonly used preset voltages for Trigger Level, TTL, CMOS (5V), CMOS (3.3V), and ECL. Users also can define their own voltage from -6.0V to 6.0V to fit with their DUT, if the number users define is not in the range, the Fig 4.5 dialogue box will appear.

Port A represents the pins from A0 ~ A7 on the signal connector of the Logic Analyzer, and so do Port B, C and D. The voltage of each port can be configured independently.

Step1. Click icon or click Trigger Property from the Trigger on the Menu Bar. The dialog box will appear as shown in Fig 4-4.



Trigger Property	×
Trigger Content Trigger Delay Trigger Range	
Trigger Level       Trigger Count         Port A       1         CMOS(5V)       2.5         Port B       ZEROPLUS Logic Analyzer         TTL       Port C         Port D       OK         User Defi       OK	
OK Cancel Default	Help

Fig 4-5 – Trigger Level Error

Step3. Trigger Count.

Type the numbers or select the number from the pull-down menu of the Count **Count T** on the Tool Bar or click the pull-down menu of the **Trigger Count** on the Trigger Property dialog box as shown in Fig 4-6. The system will be triggered at the position where the Trigger Count is set as shown in Figs 4-6, 4-7 and Fig 4-8.

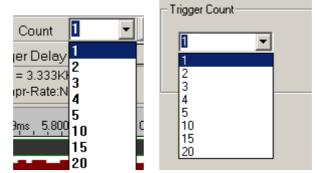


Fig 4-6 - Trigger Count Pull-down Menu

_				
			(CN01) (S/N:0000000001) - [LaDoc1]	
			. Tools Mindow Help	
- · · · · · · · · · · · · · · · · · · ·	🕰 🖗 🖓		🗓 🕨 📄 128K 🗹 👬 🖓 100MHz 💽 🟧 🗤 10%	▼ 🖗 🏟 Page  1 🔹 Count  1 💌 🗇 🗠
🛛 🖬 🕄 📐	🖑 🗰 🗍		and a bar bar bar bar bar bar	Height 30 🔻 Trigger Delay 10ns
Scale:226.192KHz				= 8.266KHz ▼ A - B = 3.333MHz ▼
Total:1.31072ms		Display	ange:-101.797465us B Pos:-120.68us  ▼ B - T :	= 8.286KHz   - Compr-Rate:No
Bus/Signal	Trigger	Filter	-79.692371u=57.587277u=35.482184u=13.37709u5 8.728003us	30. 833097us 52. 93819us 75. 043284us 97. 148377us 119. 253471u
<b>∕ A0</b> A0	<b>x</b> -	- 12		
✓ A1 A1		X		
✓ A2 A2				
🧹 A3 A3	$\boxtimes$			
✓ A4 A4		X		
<b>45</b> A5				
✓ A6 A6				
✓ A7 A7	$\boxtimes$			
<b># 80</b> 80				

Fig 4-7 – Trigger Count Screen Shot 1



🐝 ZEROPLUS-LAP-C (32128) Standard V3. 11 (CN01) (S/N:00000000001) - [LaDoc1]	
🖕 File Bys/Signal Trigger Run/Stop Data Tools Hindow Help	
🗋 😂 🗟 🎒 🍇 👯 💱 💉 👯 📲 🛐 🕨 🕪 💷 🛛 128K 💌 👫 👬 100MHz 💌 🚥 🗤 10% 💌 🤻	🛊 📣 Page 1 💌 Count 5 💌 🕾 🖻
🛛 國 🌃 🖇 🙀 🖑 🛗 📓 - 🛛 1.134396u: 🔽 🧩 🐩 💒 👫 🔛 👪 🛤 14 🕺 📓 - 🖂 🗠 He	
Scale:881.525KHz Display Post6.120118us A Post-120.98us - A - T = 8.266	
Total:1.31072ms Display Range:-22.239786us <sup>∞</sup> B Pos:-120.68us ▼ B - T = 8.286	5KHz V Compr-Rate:No
Bus/Signal Trigger Filter -16. 567805ur-10. 895824us-5. 223843u 448. 187884ns6, 120118us 11. 7920	099uz 17. 46408uz 23. 136061uz 28. 808042uz 34. 480023uz

Fig 4-8 – Trigger Count Screen Shot 2

### Step4. Trigger Page/ Delay Time and Clock

The Trigger Page and the Delay Time and Clock can't be applied at the same time.

### 1. Trigger Page:

Click **Trigger Page**, then type the numbers or select the numbers from the pull-down menu of the Page Page 1 I on the Tool Bar or click the pull-down menu of the Trigger Page on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-9, 4-10 and 4-11. The selected page numbers will be displayed on the screen.

Tip: The Trigger Bar (T Bar) will not be displayed when the setup of the Trigger Page is more than 1.

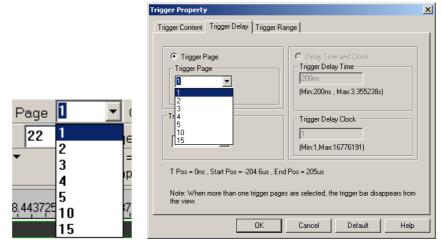


Fig 4-9 – Trigger Page

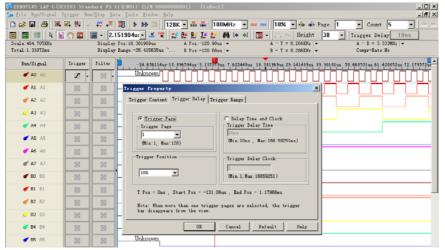


Fig 4-10 – Trigger Page and Screen (1)



				_ 🗆 ×
		Display	33         ▶ ▶ ▶         128K ➡         444         100MHZ         ▼ aver sees         1095 ➡         40 ♣         Page         5         ⊂ Count         5           151904urv	
Bus/Signal	Trigger	Filter	1, 5,1990/2ms 5,210601ms 5,221361ms 5,22212ms 5,24280ms 5,25364ms 5,264399ms 5,275159ms 5,285910ms 5,295	678ms
🝼 AO AO	Z.			<b>I</b>
🝼 A1 A1			Trigger Property	
✓ A2 A2			Trigger Content Trigger Delay Trigger Range	
🥣 A3 A3			C Brizzer Page C Belay Time and Clock	
			-Trigger Page	
🝼 AS AS			- 5 10nt 0Hin:1, Har:128) 0Hin:10ns , Har:166.59251ns)	_
🥑 A6 A6				- 1
<b>₫ А7</b> А7				
<b># 80</b> 80	×		10% (Min:1, Max:16659251)	
<b># 81</b> 81			T Pos = Ons , Start Pos = 5.11182ms , End Pos = 6.42254ms	
<b>∉ 82</b> 82			Note: Then more than one trigger pages are selected, the trigger	
🥑 <b>B3</b> B3			bur disappears from the view.	
<b>6 84</b> 84			OK Cancel Default Melp	

Fig 4-11 – Trigger Page and Screen (2)

### 2. Delay Time and Clock

Click the **Delay Time and Clock**, then type the numbers into the column of the Trigger Delay Time or type numbers into the Trigger Delay Clock at the "Trigger Delay" page of the Trigger Property dialog box as shown in Fig 4-11. Or type the numbers into the column of Trigger Delay Trigger Delay on the Tool Bar. The system will display the Start of the waveform.

- **Tip:** The formula of Delay Time and Clock is "Trigger Delay Time = Trigger Delay Clock \* (1/ Frequency)". To use the compression mode, the < Delay Time and Clock > will be unavailable.
- Step5. Trigger Position Setup

Type the percentages or select the percentages from the pull-down menu of the Bar or click the pull-down menu of the Trigger Position on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-12, 4-13, 4-14, and 4-15. The selected Trigger Position percentages will be displayed on the right side of the screen of the system.

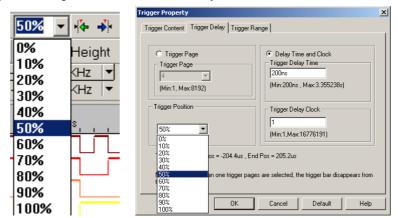


Fig 4-12 - Trigger Position Pull-down Menu

Image: Standard V3.11 (CR01)         (S/F:0000000001) - [LaBec1]           Image: Standard V3.11 (CR01)         (S/F:00000000001) - [LaBec1]           Image: Standard V3.11 (CR01)         (S/F:00000000001) - [LaBec1]						
🗅 😂 🔳 🎒 🏨	🏹 🖗 🖓	پې ب∰ ۲   2.1 Display	ta Icela findow Help			
Bus/Signal	Trigger	Filter	-43. 088083ur 32. 278562ur 21. 519041ur 10. 759521us 🐫 10 <sup>25</sup> 9521us 21. 519041us 32. 278562us 43. 088083us 53. 797604ur 🛁			
✓ A0 A0	<b>Z</b> •	- 12				
🖌 A1 A1						
✓ A2 A2	X					
🧹 A3 A3	×					
✓ A4 A4	$\boxtimes$					
<b>45</b> A5						
✓ A6 A6						
✓ A7 A7						
<b># 80</b> 80	$\boxtimes$					
<b># B1</b> B1						
<b><i>ĕ</i> 82</b> 82						

Fig 4-13 – Trigger Position 0%



🐝 ZEROPLUS-LAP-C (32	128) Stan	dard ¥3.1	1(CH01) (S/H:00000000001)	l) - [LaDoci]	
🏂 <u>F</u> ile B <u>u</u> s/Signal T	rigger Ru	n/Stop Dat	a <u>T</u> ools <u>W</u> indow <u>H</u> elp		Ð×
				👬 👬 100MHz 💌 🐅 🚥 10% 💌 🐐 🥍 Page 1 💌 Count 5 💌	h tì
🔯 🗰 💷 🔺 💱	 (*) 🗰	🚟 - 2.1	51904u: 💌 🧯 💘 📑 👪 🖁	🛿 👫 👬 🛤 le 材 📷 Herght 30 🔽 Trigger Delay 10ns -	
Scale:464.705KHz				A Pos:=120.98us ▼ A - T = 8.266KHz ▼ A - B = 3.333MHz ▼	
Total:1.31072ms		Display	Range:-35.813833us ~ B Po	8 Pos:-120.68us  ▼ B - T = 8.286KHz ▼ Compr-Rate:No	
Bus/Signal	Trigger	Filter	-25.054313u=14.294792u	'92uz-3. 535271uz 7. 22425uz 17. 98377uz 28. 743291uz 39. 502812uz 50. 262333uz 61. 021853uz 71. 78137	14us
🖌 AO 🛛 AO	<b>x</b> -	-	Unknown		ΠΙ
🝼 A1 A1	×		Unknown		
✓ A2 A2	$\boxtimes$		Unknown		
🧹 A3 A3	$\boxtimes$		Unknown		
🥑 A4 🗛	×		Unknown		
🖌 A5 A5	×		Unknown		
✓ A6 A6	$\boxtimes$		Unknown		
	$\boxtimes$		Unknown		
<b># BO</b> BO			Unknown		
<b># B1</b> B1	$\boxtimes$		Unknown		-
<b>♂ 82</b> 82	$\boxtimes$		Unknown		

Fig 4-14 – Trigger Position 10%

🚺 ZEROPLUS-LAP-C (32128) Standard V3.11 (CN01) (S/N:00000000001) - [LaDoc1]								
🏂 <u>F</u> ile Bus/Signal T	rigger Rur	√ <u>S</u> top <u>D</u> at	a Iools Window Help					
🗅 📂 🔚 🎒 🏨	🗅 😂 🗃 🎒 🎼 👯 🙀 🕫 👯 🗰 🕫 🗰 👪 🕨 🕨 🔲 128K 🚽 🆓 🖓 👘 👘 100MHz 🖃 🚥 📢 70% 🚽 🎋 Page 1 💌 Count 5 🖃 🖄 😂							
🗖 🖬 🎒 k 🕅	🖑 🗰 🛛		51904u: 🗸 🕊 🧊 👪 👪 👪 👪 🛤 10 🔸 🖉 🔪 👘 Height 🛛 👻 Trigger Delay 10ns					
Scale:464.705KHz Total:1.31072ms		Display						
Total:1.310/2ms		DISDISY	Range:=53.797604us ~ B Pos:=907.11us - B - T = 1.102KHz - Compr-Rate:No					
Bus/Signal	Trigger	Filter	ڬ –43. 038083u=32. 278562u=21. 519041u=10. 759521us 💀 10. 759521us 21. 519041us 32. 278562us 43. 038083us 53. 797604u					
<b>✓ A0</b> A0	<b>7</b> -	- 12						
🝼 A1 A1	$\otimes$							
✓ A2 A2			Unknown					
🧹 A3 A3			Unknown					
✓ A4 A4			Unknown					
<b>45</b> A5	×		Unknown					
<b>46</b> A6			Unknown					
✓ A7 A7	X		Unknown					
<b>Ø BO</b> BO			Unknown					
<b># B1</b> B1			Unknown					
	×		Unknown					

Fig 4-15 – Trigger Position 70%

### Step6. Trigger Range Setup

Click **Trigger Property** from the Trigger on the Menu Bar. Then, Click the Trigger Range, the dialog box will appear as shown in Fig4-16.

**Tip**: This function is mainly for the range control for the saved files after triggering. According to the procedures of the range control, users can start the save of data according to the requirement of its time and times to get the standard of data statistic status.

Trigger Property	×
Trigger Content Trigger Delay Trigger Range	
Range Setting	
Time Sample 🔽 1	ninute
OK Cancel	Default Help

Fig 4-16 - Trigger Range

- 1. Trigger Range: The default is not activated.
- 2. There are "Time Sample" and "Frequency Sample" in the part of Range Setting; the default is "Time



Sample". The units of Time Sample are 'second', 'minute', 'hour' and 'day'. The unit of Frequency Sample is 'times'. Users can set the value by themselves in the editor box.

### Task 3. Bus Trigger and Trigger Mark Setup

Step1. Click 🐺 icon or click Bus Trigger Setup and Trigger Mark from the Trigger on the Menu Bar. The menu is shown as Fig 4-17.

₽₽ ₽Ţ ₽Î İT	Bus Trigger Setup Channel Trigger Setup Trigger Property Trigger Mark Pulse Width Trigger Module(Option)
$\boxtimes$	Don't Care
	High
	Low
20	Rising Edge
50	Falling Edge
Х	Either Edge
	Reset

Fig 4-17 -Trigger Menu

- Step2. Bus Trigger Setup
  - 1. Bus Trigger Setup

p			
Bus Trigger			×
Bus Trigger Protocol A	nalyzer Trigger		
•			
Bus Name	Operator	Value	
Bus1 👻	=	■ 35	
- Data Format			
C Binary	O Decimal	C Decimal(Signed)	
Hexadecimal		C Gray Code	
	- Abdi	Code anay code	
C Complement			
OK	. Canc	el Default	Help

Fig 4-18 - Bus Trigger Dialog Box

**Tip:** The Bus Name item can be selected from the pull-down menu (It only displays the Bus name), and also the Decimal(signed), Gray Code and Complement Modes are added.

### 2. Protocol Analyzer Trigger Setup

**Tip:** This function can be used in the Modules, LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A LAP-321000U-A, LAP-C(16032), LAP-C(16064), LAP-C(16128), LAP-C(162000), LAP-C(32128) and LAP-C(321000) after registering. And for the LAP-322000U-A and LAP-C(322000), it is not necessary to register as they can be used for free. Before registering, the button "OK" in the Protocol Analyzer Trigger dialog box is the button, "Register"; when users press this button, Register, a Register dialog box will pop up. Then users need to enter the correct Register Code so that they can use this function, Protocol Analyzer Trigger.



Bus Trigger Protocol Analyzer Trigger           Image: Protocol Analyzer Trigger           Protocol Analyzer: Protocol Packet: Value:	us Trigger			×
	Bus Trigger Protocol And	alyzer Trigger		
Protocol Analyzer: Protocol Packet: Value:	📕 Allow Protocol Ana	yzer Trigger		
	Protocol Analyzer:	Protocol Packet:	Value:	
Data Format C Binary C Decimal C Decimal(Signed) C Hexadecimal C ASCII C Gray Code C Complement			<ul> <li>Binary</li> <li>Decimal</li> <li>Decimal(Signed)</li> <li>Hexadecimal</li> <li>ASCII</li> <li>Gray Code</li> </ul>	
OK Cancel Default Help	ОК	Cancel	Default Help	

Register Dialog Box:

Register		×
The function is an optional purchased ite activate this function for your necessary.		
Enter serial key:		
	ns about ordering software please follow the team will respond to your enquiry as soon as	
>> By phone:	886-2-66202225	
>> Applications through Email:	service_2@zeroplus.com.tw	
>> Website:	http://www.zeroplus.com.tw	
Copyright(C) 1997-2011 ZEROPLUS TECH	HNOLOGY CO.,LTD.	
	OK Cancel	

Bus Trigger		×
Bus Trigger Protocol An	alyzer Trigger	
Allow Protocol Ana Protocol Analyzer:		Value:
Bus1(I2C)     Bus1(I2C)     Substant     Substan	Start C ADDRESS C Read C Write A-ACK A-ACK A-NACK DATA D-ACK C D-ACK C D-NACK Stop REG ADDR	Data Format C Binary C Decimal C Decimal(Signed) G Hexadecimal C ASCII C Gray Code C Complement
OK	Cancel	Default Help

Fig 4-19 -2 After Registering

Allow Protocol Analyzer Trigger: When it is selected, the Protocol Analyzer Trigger function is activated. And then users can set Protocol Analyzer, Protocol Packet, Value and Data Format.

② 孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

Protocol Analyzer: It only displays the name of Protocol Analyzer and only one name can be selected.

Protocol Packet: It is displayed according to the packet in every protocol analyzer.

**Value**: The value needs to be entered in the frame, and the data mode can be selected by users according to their requirements; the default is Hexadecimal! When a value can be input in the selected protocol analyzer data, the frame can be enabled! Or, the frame will be disabled! For example: Protocol Analyzer I2C, when the protocol packet is DATA, the frame can be used; to the contrary, when the protocol packet is START, the frame is disabled.

**Data Format**: The displayed value mode can be selected! There are five options: Binary, Decimal, Decimal(signed), Hexadecimal, ASCII, Gray Code and Complement.

### Step3. Trigger Mark Setup

To find the item in the Bus better, users can activate the Trigger Mark function after starting Bus Trigger; the trigger mark is shown with T bar. According to the number of the trigger position, the T bar is displayed in order T0, T1, T2, T3, T4...and the color is red as the image below:

1. Bus: The trigger condition is "0"; the red T bar displays the trigger condition in order.

Bus/Signal	Trigger	Filter	<b>P</b>	-1.833	0.667	3.167 5.66	57	167 10	. 667 1	3, 167	15.667	8. 167
Bus1	OX0 🗸		know (0X4	a)	1)	0X0	XOX1	0X0 0X4	XOXDX	OXC	0X4 0X5 0X4	OXC
• A0 A												
●A1 A	Ē							_				
● A2 A	E	$\boxtimes$										
<mark>.</mark> A3 A												1
🥑 A4 A4												1

Fig 4-20 - Bus Trigger Mark

2. Protocol Analyzer (I2C): The trigger condition is "Data=0"; the red T Bar displays the trigger condition in order.



Fig 4-21 - Protocol Analyzer Trigger Mark

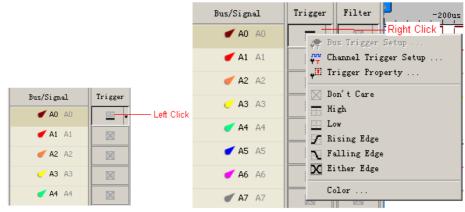
Tip: The Trigger Mark function is available for the LAP-322000U-A , LAP-C(162000), LAP-C(322000) Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A, LAP-321000U-A, LAP-C(16032), LAP-C(16064), LAP-C(16128), LAP-C(32128) and LAP-C(321000) Modules.



### Task 4. Bus/Signal Trigger Condition Setup

Highlight a designated signal, and then set its required trigger condition.

- 1. Left click III to set the signal trigger condition as shown in Fig 4-22.
- 2. Right click is to set the signal trigger condition as shown in Fig 4-23.
- 3. Click **Trigger** on the Menu Bar and choose a trigger condition from the list of triggers as shown in Fig 4-24.



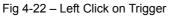


Fig	1_23 _	Right	Click	on	Trigger
FIY *	+-20 -	RIYIIL	CIICK	UII	niyyei

nn T T	Bus Trigger Setup Channel Trigger Setup Trigger Property
$\mathbb{X}$	Don't Care
	High
	Low
7	Rising Edge
30	Falling Edge
х	Either Edge
	Color

Fig 4-24 – Trigger Menu



### Task 5. Run to Acquire Data

### 1. Single Run

Click the Single Run icon from the Tool Bar or press **START** button on the top of the Logic Analyzer (or press F5), then activate the signal from the DUT to the Logic Analyzer to acquire the data shown in the waveform display area.

### 2. Repetitive Run

Click the Repetitive Run *icon* from the Tool Bar, then activate continuous signal to the Logic Analyzer to acquire the repetitive data, and then click the Stop **i** icon to end the repetitive run.

Tip: Click 📓 icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

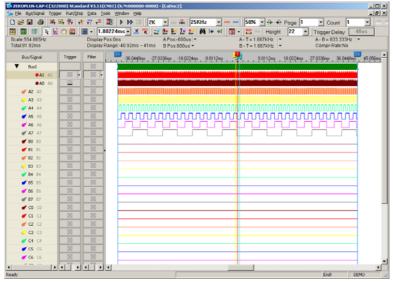


Fig 4-25 – Click 📓 Icon to View All the Data

### 3. Stop to end Run

Click the Stop <a>[</a> icon to end the Run.

**Tip:** If the status is "Waiting..." with no signal outputting as shown in Fig 4-26, click the Stop icon to end the Run; check the setup again, and try the run process again.

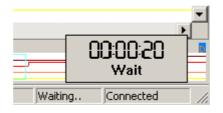


Fig 4-26 - Waiting Status



# 4.2 Bus Logic Analysis

Section 4.2 presents detailed instructions about logic analysis with a set of grouped signals, which is known as Bus Logic Analysis.

Basic Software Setup of the Bus Logic Analysis

- Step1. Set up the RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Group signals into a Bus

Click **Channels Setup** on Bus/Signal of the menu bar, or click icon. The dialog box shown in Fig 4-27 will appear.

Signal Fill		4		1		ód D	in/S	igna	(	ß	De	÷.	1.77	53	91	11	2	Dek	ka I	4		F	ker	tore	Dief	a.k							
Group int	Part		-	-	Pa	D		-			-	+	51	2	-	-	-			7	-		-	-		-	-		tat.	A:	-	-	
Ungroup	Ti Condition	1000	8				ŝ	1		8	8	ŝ	8	100	20	8			8	8		3	100	8	8	1	1	1000	1000			8	
100000	Bus1	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	2	2		
Expand	A2 A3	Ę	2	2	4	공	룅	-	-	4	\$	2	4	3	Ş.	÷	0	7	ş	2	4	3	ŝ	1	0	7	2	2	4	2	4	1	0
Colleges	A4	17	10	5	÷	5	21	÷1	ő	Ŷ	-	ŝ	4	5	5	÷.	0	5	2	5	4	5	2	÷	0	2	6	5	10	5	2	1	ő
Collapse	A4 A5	7	6	5	4	3	2	1	0	7	6	5	4	3	2	t	0	7	6	5	4	3	2	1	0	7	6	1	4	3	2	1	0
and a second sec	A6	7	- 6	5	4	3	2	1	0	7	ñ	5	4	3	2	1	0	7	÷	5	4	3	2	1	0	7		5	4	3	2	1	0
Format R	A7.	7	5	5	4	21	2	1	0	7	5	5	4	3	2	1	0	7	6	5	4	3	2	1	2	12	5	5	4	3	2	1	0
	80	17	1.6	2	4	2	2		0	7		9	4	83	2		0	7		2	4	2	2	1		7		. 5	14	2	2	1.12	0
Rename	Assignment Court	1		3	1		100	10	1	1	1	1	1	1	1	3	1	1	1		4	1	1	1		1	1					1	1

Fig 4-27 – Channels Setup

Rename the Bus and set up the channels of the Bus as shown in Fig 4-28.

Port				Po	rt E			F	Port /	4			
Tr.Condition		$\otimes$	$\otimes$	$\otimes$	$\sim$		$\mathbb{X}$	$\mathbb{X}$	$\mathbb{Z}$	$\mathbb{Z}$	$\mathbb{X}$	$\mathbb{X}$	
Fi.Condition	X	X	$\mathbb{X}$	$\mathbb{X}$	$\sim$								X
Bus1	7	6	5	4	З	7	6	5	4	3	2	1	0
A2	7	6	5	4	З	7	6	5	4	3	2	1	0
A3	7	6	5	4	З	7	6	5	4	3	2	1	0
A4	7	6	5	4	З	7	6	5	4	3	2	1	0
Bus2	7	6	5	4	З	7	6	5	4	3	2	1	0
A6	7	6	5	4	З	7	6	5	4	3	2	1	0
A7	7	6	5	4	З	7	6	5	4	3	2	1	0
B0	7	6	5	4	З	7	6	5	4	3	2	1	0
Assignment Count	1	1	1	1	1	1	1	1	1	1	1	1	1

Fig 4-28 – Rename Bus

- 1. Click the column, then type the given name of the Bus, and then press Enter to confirm it.
- 2. Go to the relative channels as shown in the example and go to numbers 0, 1, 2, 3, which are located on column A and row Bus1. Click them to become purple, then set these segments of channels.
- 3. Click **OK** to get the result as shown in area 1.

	孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.
/	Zeroplus Technology Co., Ltd.

	<b>AO</b> AO	-					4dd B	ius/S	ignal		20	elete	BUS		d.		۵	elete	AI			Rest	ore (	Defau	ts	$\mathcal{V}$				
-	Service Street		Port			Po	at D		_	1		<u>र</u>	Port	С	-	-		_	j.	Port	3		_		-		Port /	A.	_	5
	A2 A2		Tr.Condition	X	29.1	× 18	20	X	89	×		0.00	24		×	28	24 8	A A	125	50	X	×	X)	X 2	9 P	<u>a 18</u>	24	LEI	20	5
C	Bus1 A3	<	Freenation	201	~		101	5						101	101	KOC.		7 0		109	101	2		a   -			1051			5
•	A4 🔒	1 (	AO	7	6	5 4	3	2	1	0	7 6	5 5	4	3	2	1	0	7 6	5	4	3	2	1	0	1	6 5	4	3	2 1	0
- 682	AO	AO	A2 Burg	7		54 54	3	2	1	7	7678	5 5	4	3	2	1	0	76 76	5	4	3	2	1	0 1	7 8	5 5 5 5	4	3	2 1	0
		Ĩ	A4 A5	7	6	5 4	3	2	1	0	767	5 5	4	3	2	1	0	7676	5	4	3	2	1	0	78	5 5	4	3	2 1	0
	• A1	41	A6	7	6	5 4	3	2	1	0	7 8	5	4	3	2	1	0	7 6	5	4	3	2	1	0		5 5	4	3	2 1	0
	<b>e</b> A2	42	A7	7	6	5 4	3	2	1	0	7 8	5 5	4	3	2	1	0	7 6	5	4	3	2	1	0		5 5	4	3	2 1	9
	C A3	43	Count								177																1			•
	O A4	A4	Reserve	umetr	rm d	ata ar	d she	ow th	em.																			-		

Fig 4-29 - Channels Setup Window

#### Tip: Channels Setup

In the dialog box of Channels Setup, there isn't only Add Bus/Signal, but also Delete Bus/Signal, Delete All, Restore Defaults provided.

- 1. Delete Bus/Signal: Firstly highlight the Bus or channels on area 6 of Fig 4-29, then click **Delete Bus/Signal** to delete them.
- 2. Delete All; Click Delete All to delete all Bus/signals on area 6 of Fig 4-29.
- 3. Restore Defaults: Click **Restore Defaults** to restore the dialog box of Channels Setup as shown in Fig 4-27.

#### Step3. Trigger Condition Setup

1. Highlight the Bus which will be triggered then click 📌 icon or select **Bus Trigger Setup** from the Trigger of the Menu Bar, the dialog box as shown in Fig 4-30 will appear.

Bus	Trigger			×
В	us Trigger Protocol A	nalyzer Trigger		
	Bus Name	Operator	Value	
	Data Format	C Decimal	C Decimal(Signed)	
	Hexadecimal	O ASCII	🔘 Gray Code	
	C Complement			
	OK	Cano	cel Default	Help

Fig 4-30 – Bus Trigger Setup

Tip: Left click on Trigger column of the Bus as shown in Fig 4-31.

Trigger	
	Single Click
$\square$	
$\square$	

Fig 4-31 – Trigger Column



- 2. Set Binary, Hexadecimal, Decimal, Decimal (signed), ASCII, Gray Code or Complement as the Data Format of the Bus to represent the value (see Fig 4-30).
- 3. Set "=" and "Don't Care", and type the value of the Bus into Value column to set the trigger condition of the Bus.
- 4. Click **OK** to confirm the settings.
- **Step4.** Click **Run** and activate the signal from the tested board to the system to get the result as shown in Fig 4-32.
  - **Tip:** Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms. Set **Value** is "2" as Hexadecimal, and set **Operator** equals to "=", then click **OK**. Click **Run** and activate the signal from the tested board to the system to get the result as the trigger happens on 0X2.

🏡 <u>F</u> ile B <u>u</u> s/Signal	Trigger	Run/Stop	Data Tools Mindow Help[27]
🗋 😹 🖥 🎒	ų 🔀 🆗	Ŷ₽ ŶŦ ¥	🇯 🧾 🕨 🕪 🗆 🛛 2K 💌 🚧 🚺 100MHz 💌 🛲 50% 💌 🎋 🎝 Page 1 💌 Count 1
高高 ( 1 1 1			
🐹 🔠 🚺 🔖	📓 🖤 🗰	×	10ns 🔽 🧩 💏 🔛 🔛 🔛 🗱 👬 🏘 🍬 🖓 🚯 🗸 🔡 📩 Height 🛛 30 🔽 Trigger Delay 📃
Scale:27.5301532 Total:131072			(P0s:343)         A P0s:64527   ▼         A - T = 64527   ▼         A - B = 30   ▼           (Range: 345 ~ 1034)         B P0s:64497   ▼         B - T = 64497   ▼         Compt-Rate.No
Bus/Signal	Trigger	Filter	📙 , -207.465 , -69.815 📕 67.836 , 205.487 , 343.138 , 480.788 , 618.439 , 756.09 , 893.741 , 1031.391 🚆
▼ Bus1	0X2 🔻	-	0x3 (0x2) 0x0 (0x1) 0x3 0x1 (0x0) 0x2 0x0 (0x1) 0x3 (0x1
•A0 A0			Bus Trigger
🝼 A1 A1			Bus Trigger   Protocol Analyzer Trigger
🥑 A2 A2			Bus Name Operator Value
🥑 A3 A3	$\boxtimes$		Busi V = 2
🥑 A4 A4			Data Format
🝼 A5 A5	$\square$		C Binary C Decimal C Decimal (Signed)
🥑 A6 A6	$\square$		© Hexadecimal C ASCII C Gray Code
✓ A7 A7	$\square$		C Complement
<b>e BO</b> BO			
🥑 B1 B1	$\square$		
🥑 B2 B2			OK Cancel Default Help

Fig 4-32 – Bus Trigger Setup

# 4.3 Plug Analysis

### **Plug Introduction**

Protocol Analyzer operates in the form of Plug; every Protocol Analyzer has a plug, per plug is independence modularization. One Protocol Analyzer plug can analyze many Buses at the same time, however, because the independence of every plug, the Protocol Analyzer plug only supports I2C, UART, SPI, HDQ, 1-WIRE, CAN 2.0B at present. In the future, it will support more Buses, and when the Protocol Analyzer renews, it only needs to download the new Protocol Analyzer plug to cover the old Protocol Analyzer plug; the speed is very fast.

Operating Instructions: There are PlugIns data file in the position of installing LA software. All Protocol Analyzer plugs which are used at present are put in the data file, the DLL file can be added or deleted in the content, and in the Bus property, all Protocol Analyzer plugs that can be used at present can be seen as the figure below:



PluginsA		_ @ ×
Als tel New Peverts	i tedi pen	EÎ.
4+ teck + + + - 1 2	seech Circles Gestary 在行义の 田·	
Address 🗋 PlugErsA		<u>.</u> 2°60
PlugInsA	କ୍ତି କି କି କି କି Nation Region Region and Region and Angel 	
Select an ten to view its description.		
See also: <u>Hy Documents</u> <u>Hy Network Places</u> Hy Computer		

#### Fig4-33 - PlugInsA

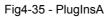
C Bus	Color Config
Activate the Latch Function	A0 👻
	Rising Edge 💌
Protocol Analyzer Setting	
Protocol Analyzer     ZEROPLUS LA 1-WIRE MODULE V1.10.00     ZEROPLUS LA 2 WIRE MODULE V1.10.00	
	(CN01) (CN01) N01) DULE V1.51.00(CN01) 01) 00(CN01) 0(CN01) E V1.01.00(CN01) D0.00(CN01)

#### Fig4-34 - Bus Property

Every Logic Analyzer Module can provide some basic Protocol Analyzer plugs. When users need to use the analysis which is not provided by the basic Protocol Analyzer plugs, you can purchase from our company, and then, you can get this Protocol Analyzer plug and the register code.

STEP 1. Put the CAN 2.0B Plug in the PlugIns as the Fig4-35.

🔄 PlaglinsA		_ 9 ×
File Ecit Wext Favorite	es Teals Help	12
4-Back + + - 🖬 🔞	(Seach 已Fiders ③Haday   復 聖 X 29   田•	
Address 🖸 Ruginsa		· 1960
PlugInsA Select an ter to view its description. See elso: My foncurrents My foncurrents My foncurrents My foncurrents My foncurrents	କ୍ତି କ୍ତି କ୍ତି କ୍ତି କ୍ତି RigtWREd RigtWRE.d RigtWated	





STEP 2. Select CAN 2.0B in the Protocol Analyzer list.

Bus Setting	
C Bus	Color Config
Activate the Latch Function	
	<u>_</u>
	Rising Edge
Protocol Analyzer Setting	
Protocol Analyzer	Parameters Config
ZEROPLUS LA CAN 2.08 MODULE V1.32.00(	
C ZEROPLUS LA I2C(EEPROM 24LC561/24LC5	62) MODULE V1.00.00(CN01)
© ZEROPLUS LA I2C MODULE V2.01.03	upp)
C ZEROPLUS LA LG4572 MODULE V1.00.00(CI	
C ZEROPLUS LA LG4572 MODULE V1.00.00(CI C ZEROPLUS LA PECI MODULE V1.11.00(CN0)	1)
<ul> <li>⊂ ZEROPLUS LA LG4572 MODULE V1.00.00(CI</li> <li>⊂ ZEROPLUS LA PECI MODULE V1.11.00(CN0)</li> <li>⊂ ZEROPLUS LA PT2262/PT2272 MODULE V1.</li> </ul>	1) 00.00(CN01)
C ZEROPLUS LA LG4572 MODULE V1.00.00(CI C ZEROPLUS LA PECI MODULE V1.11.00(CN0)	1) 00.00(CN01)
<ul> <li>⊂ ZEROPLUS LA LG4572 MODULE V1.00.00(CI</li> <li>⊂ ZEROPLUS LA PECI MODULE V1.11.00(CN0</li> <li>⊂ ZEROPLUS LA PT2262/PT2272 MODULE V1.1</li> <li>⊂ ZEROPLUS LA S2CWire/AS2CWire MODULE V1.1</li> </ul>	1) 00.00(CN01) /1.00.00(CN01) )1)

Fig4-36 - Bus Property

STEP 3.Click Parameters Configuration button, select Register and enter the Serial Key.

PROTOCOL ANALYZER CAN 2.0B		×
Configuration   Packet   Data Format	Register	
	oding function is an optional purchased ey to activate this function for your necessary.	
· · · · · ·	· · · · ·	
Enter serial key:		
	tions about ordering software please follow the les team will respond to your enquiry as soon as	
>> By phone:	886-2-66202225	
>> Applications through Email:	service_2@zeroplus.com.tw	
>> Website:	http://www.zeroplus.com.tw	
Copyright(C) 1997-2010 ZEROPLUS	TECHNOLOGY CO.,LTD.	
	Register Cancel Default	Help

Fig4-37 - Protocol Analyzer CAN 2.0B Register dialog box



## 4.4 Bus Packet List

Bus Packet List is a graphics list which is used for doing Statistics and showing Bus Packet List. It is visual and direct, especially for I2C, USB 1.1 and CAN 2.0B. When there is a packet list, it gets twice the result with half the effort to check the data. Packet List has its startup button in Toolbar. After starting it, it will show a small window under the waveform window. Users can alter its size to find more data.

Notice: If you want to learn more about the Bus Packet List, please refer to the Specification of the Protocol Analyzer.

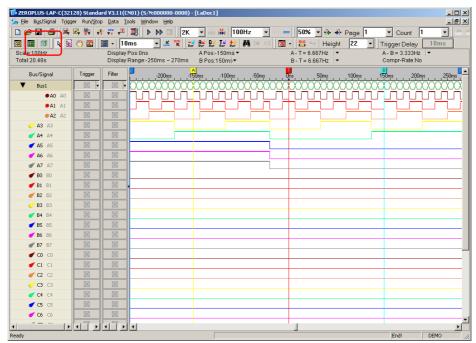


Fig 4-38 - Packet Icon

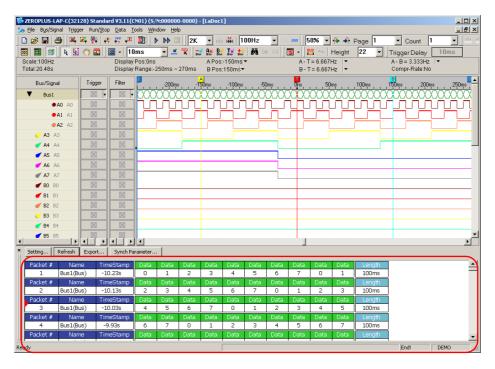


Fig4-39 - Bus Packet List

Packet List has a setup window; users can set up the Packet List according to their requirements. Setting



Bus Packet Length in dialog box is only used for doing Bus Statistic. Users can define how long the time is as a data packet to add the export function. See the following figure.

Setting			×
Bus Select	Data Format		7
✓Bus1(Bus)	C Binary	O Decimal	
	C Decimal(Signed)	• Hexadecimal	
	C ASCII	🔘 Gray Code	
	C Complement		
	-Bus Packet Length		1
	100mg	in: 10ms ax: 20.48s	
Packet Item Packet  Name	Z TimeStamp Len	oth Data	]
	ninestanip terr		
• • • • • • • • • • • • • • • • • • •	kt Color Auto		
ОК	Cancel Defaul	t Help	

Fig4-40 - Packet List Setting

ietting	Refresh Expo	ort Synch Pa	arameter											
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	

Fig4-41 - Bus Packet List

1. View Specifications

Packet #, Name and TimeStamp can be selected to display from the Packet List Setting dialog box.

Packet #: List the order of Packet.

Name: Display the name of Packet, or the Filter Display Bar.

TimeStamp: It is the starting point of the Packet.

Tip: The rest name and content are supplied by Plug.



<b>×</b> 	Setting	Refresh Expo	rt Synch Pa	rameter													
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	1	Bus1(I2C)	-1us	50	Write	A-ACK	00	D-ACK	75	D-ACK	01	D-ACK	23	D-ACK	45	D-ACK	
	DA 6																
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK							
	2	Bus1(I2C)	10.2064ms	50	Write	A-ACK	00	D-ACK	75	D-ACK							
	Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-NACK	DESC								
	3	Bus1(I2C)	10.2982ms	50	Read	A-ACK	01	D-NACK	DATA	NACK							
	Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA				DATA	D-NACK	DESC				
	4	Bus1(I2C)	10.3554ms	50	Read	A-ACK	23	D-ACK	45	D-ACK	67	D-NACK	DATA N	IACK			
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	5	Bus1(I2C)	20.477ms	50	Write	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-ACK	J
	E																•

Fig4-42 - Protocol Analyzer I2C Packet List

Setting: It is used to open Packet List Setting dialog box.

Refresh: Press this button, the list view can renew automatically.

Export: Export the workspace into Text (\*.txt) and CSV Files (\*.csv).

Synch Parameter: Open the synch parameter setting dialog box and activate the packet and waveform synch function.

2. Display Protocol Analyzer Packet in Order

Tip: The below view are Protocol Analyzer I2C; the packet is determined by the position of the TimeStamp.

× ∥	Setting	Refresh Exp	ort Synch Pa	ameter													
	Packet #	Name	TimeStamp	4.DDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	1	Bus1(I2C)	-1us	50	Write	A-ACK	00	D-ACK	75	D-ACK	01	D-ACK	23	D-ACK	45	D-ACK	
	6		]					_			_						
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK							
	2	Bus1(I2C)	10.2064ms	50	Write	A-ACK	00	D-ACK	75	D-ACK	J						
	Packet #	Name	TimeStamp	4.DDRESS	Read	A-ACK	DATA	D-NACK	DESC	RIBE							
	3	Bus1(I2C)	10.2982ms	50	Read	A-ACK	01	D-NACK	DATA	VACK							
	Packet #	Name	TimeStamp	4.DDRESS	Read	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-NACK	DESCR	RIBE			
	4	Bus1(I2C)	10.3554ms	50	Read	A-ACK	23	D-ACK	45	D-ACK	67	D-NACK	DATA N	<b>I</b> ACK			
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	5	Bus1(I2C)	20.477ms	50	Write	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-ACK	1
	DA	TA D-ACK		,					,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	PAR						DHOR	J



Tip: When the Display Bar of Signal Filter is activated, the Bar should be displayed in the Bus Packet List, and also the TimeStamp, ADDRESS and length of the Bar will be displayed.

3. Packet Idle and Packet Length

Packet Idle: Packet interval time Packet Length: Packet time length

When those above two items are to be displayed, it only chooses one of them to display, which is controlled by Plug.

Because it is impossible that every Protocol Analyzer packet has registered timestamp and end, we add two special Unknow\_Flag to judge the timestamp and end of the packet which are Unknow \_Start\_Flag and Unknow\_End\_Flag.



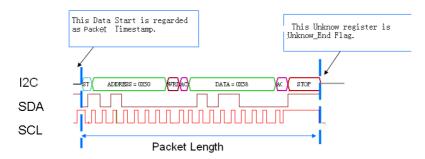


Fig4-44 - Protocol Analyzer I2C Packet Length

Tip: Because I2C has started as the Packet TimeStamp, it does not need to use Unknow\_Start\_Flag as the start.

4. Bus

Setting	Refresh Expo	ort Synch Pa	arameter										
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
4	Bus1(Bus)	-9.93s	6	7	0	1	2	З	4	5	6	7	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
5	Bus1(Bus)	-9.83s	0	1	2	3	4	5	6	7	0	1	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
6	Bus1(Bus)	-9.73s	2	3	4	5	6	7	0	1	2	3	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
7	Bus1(Bus)	-9.63s	4	5	6	7	0	1	2	3	4	5	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length

Fig4-45 - Bus Packet List

Packet Length and Packet Idle Length

Packet's TimeStamp is the start of Bus Data; the default length is controlled by the setting dialog box. If the input packet length isn't the end of data. The software will prolong the length of Packet to end the data automatically as the figure below.

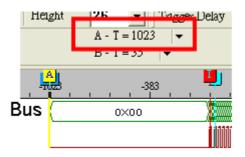


Fig4-46 - Auto-Prolong Packet

The Fig4-46 is a Bus; its first data is 0x00, and its length is 1023. If users input 20 as the Bus length. But 20xaddress is not the end of this data, so the software will prolong the length of the Packet to 1023 automatically.



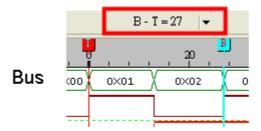


Fig4-47 - Packet End

The Fig4-47 is a Bus. If the Start of the packet is T bar and the set Bus length is 20, but the data 0x02 isn't the end, at that time, the Packet will be prolonged to the end dot automatically, that is to say, the Address 27 (B bar ) is the End of the packet.

The above two data are made consecutively as the figure below.

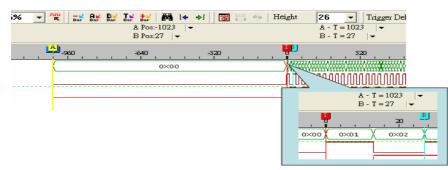


Fig4-48 - Auto-Prolong Packet

The Packet List is displayed as the figure below:

Setting	Refresh Expo	ort Synch Pa	rameter											
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	З	4	5	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
5	Bus1(Bus)	-9.83s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
6	Bus1(Bus)	-9.73s	2	3	4	5	6	7	0	1	2	3	100ms	

Fig4-49 - Bus Packet List

**Tip:** The Protocol Analyzer Packet will be explained in the following plug.

5. Packet and Waveform Synchronization

For the convenience of fast corresponding between packet data and waveform data, and what is more, in order to make it easier for users to look up data, we add the Packet and Waveform Synchronization function.

In order to operate conveniently, we add a Synch Parameter button on the BUS Packet List as the image below:

Setting	Refresh Expo		rameter	-										
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms	]
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
5	Bus1(Bus)	-9.83s	0	1	2	3	4	5	6	7	0	1	100ms	]
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
6	Bus1(Bus)	-9.73s	2	3	4	5	6	7	0	1	2	3	100ms	

Fig 4-50 - Synch Parameter on the BUS Packet List

At the same time, a Synch Parameter Setting dialog box is added.

Synch Parameter Setting	×
Activate Packet and Waveform	Synch
Synch Point of Packet List	Synch Point of Waveform Area
🕞 Тор	C Left
C Middle	<ul> <li>Middle</li> </ul>
	OK Cancel

Fig 4-51- Synch Parameter Setting Dialog Box

Activate Packet and Waveform Synch: The default is not activated.

**Top**: When the Packet and Waveform Synch is activated, the synch point in Packet List is the top packet segment which is displayed by list.

**Middle**: When the Packet and Waveform Synch is activated, the synch point in Packet List is the middle packet segment which is displayed by list.

**Left**: When the Packet and Waveform Synch is activated, the synch point in the waveform area is the left packet segment which is displayed by waveform.

**Middle**: When the Packet and Waveform Synch is activated, the synch point in the waveform area is the middle packet segment which is displayed by waveform.

Activate Packet and Waveform Synch, select Top and Left.

Synch Parameter Setting	×
Activate Packet and Waveform	Synch
Synch Point of Packet List	Synch Point of Waveform Area
🖲 Тор	• Left
C Middle	O Middle
	OK Cancel

Fig 4-52 - Synch Parameter Setting Dialog Box



-			
	-	1(CN01) (5/N:00000-0000) - [I2C]	<u>_   ×</u>
🏂 File Bys/Signal Trigge			
		1.450216u 🛫 💒 🎇 🔜 🎎 🔛 ፲৯ 🔝 👪 🛤 🗠 🕬 🔞 🐨 👘 Height 22 📼	Trigger Delay 200ns
Scale:689.552KHz Total:78.6034ms		lay Pos:32.654543us A Pos:-52.0884ms ▼ A - T = 19.198Hz ▼ lay Range:-3.600865us ~ B Pos:-52.0824ms ▼ B - T = 19.2Hz ▼	A - B = 166.667KHz ▼ Compr-Rate:191.903
Bus/Signal	Trigger Filter		15 00 05
			15 20 25
	× ×		
SCL A0			
A2 A2			L
A3 A3			
A4 A4			
✓ A5 A5			
✓ A6 A6			
✓ A7 A7			
<b>Ø BO</b> BO			
<b><i>ĕ</i> <b>B</b>2 B2</b>			
🥑 B3 B3			
🍼 B4 B4			
<b>₹ №7 №7</b>			
× Setting Refresh	Export Synch	Parameter	
Packet # Nam	ne TimeStamp	ADDRESS Write A-ACK DATA D-ACK DATA D-ACK DATA D-ACK DAT	A D-ACK DATA D-ACK
1 Bus1(I2	C) -1us	50 Wine A-ACK 65 D-ACK 75 D-ACK 01 D-ACK 23	D-ACK 45 D-ACK
DATA D-A			
67 D-A Packet # Nam		ADDRESS Write A-ACK DATA D-ACK DATA D-ACK	
2 Bus1(I2		50 Write A-ACK 00 D-ACK 75 D-ACK	
Packet # Nam	ne TimeStamp	ADDRESS Read A-ACK DATA D-NACK DESCRIBE	<b>T</b>
Ready	<u> </u>		End! DEMO

Display the corresponding waveform and packet as below image:

Fig 4-53 - Waveform and Packet Synchronization Interface



# 4.5 Bus Analysis

The setup is correlated to the Bus which needs to be made up, for example: Bus, Protocol Analyzer. Open the dialog box:

STEP 1.Click Tools on the Menu Bar, and then select Bus Property or select is to set up Bus Property.



Fig4-54 - Bus Property on Menu Bar

Fig4-55 - Bus Property on Tool Bar

STEP 2.Click the **Right Key** on the Bus/Signal column, and then select **Bus Property**.

Tip: The signals must be grouped into Bus, or the Bus Property can not have effect.

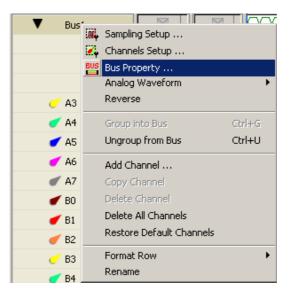


Fig4-56 - Right Key to Set Bus Property



### 4.5.1 Bus Analysis

The Bus Analysis function enables the system to analyze the Bus.

Basic Software Setup for the Bus

STEP 1. Click **Bus Property**, the following dialog box will appear.

Protocol Analyzer Setting	Color Config
Protocol Analyzer Setting  Protocol Analyzer  C Protocol Analyzer  C ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01)  C ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01)	ising Edge
Protocol Analyzer Setting  Protocol Analyzer  C Protocol Analyzer  C ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01)  ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01)	
Protocol Analyzer      ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01)     ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01)	Parameters Config
ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01)	Parameters Config
C ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01)	<b>_</b>
ZEROPLUS LA ARITHMETICAL LOGIC MODULE V1.51.00(     ZEROPLUS LA ARITHMETICAL LOGIC MODULE V1.51.00(     ZEROPLUS LA BUS MODULE V1.00.00(CN01)     ZEROPLUS LA CAN 2.0B MODULE V1.32.00(CN01)     ZEROPLUS LA CCIR656 MODULE V1.31.00(CN01)     ZEROPLUS LA COMpact Flash 4.1 MODULE V1.01.00(CN01)     ZEROPLUS LA CMOS IMAGE MODULE V1.00.00(CN01)	
Use the DsDp	Find

Fig4-57 - Bus Setting

STEP 2. Click Color Configuration to set **Bus Data Color**.

Bus Property	×
Bus Setting	
<ul> <li>Bus</li> </ul>	Color Config
Activate the Latch Function	AO
	Rising Edge
Protocol Analyzer Setting	
O Protocol Analyzer	Parameters Config
CZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01) ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01)	<u> </u>
C ZEROPLUS LA AC97 MODULE V1.02.00(CN01)	
C ZEROPLUS LA ARITHMETICAL LOGIC MODULE V1.51.	00(CN01)
C ZEROPLUS LA BUS MODULE V1.00.00(CN01) ZEROPLUS LA CAN 2.0B MODULE V1.32.00(CN01)	
C ZEROPLUS LA CCIR656 MODULE VI.32.00(CN01)	
C ZEROPLUS LA Compact Flash 4.1 MODULE V1.01.00(0	INO1)
C ZEROPLUS LA CMOS IMAGE MODULE V1.00.00(CN01)	<b>T</b>
Use the DsDp	Find
More Protocol Analyzer	
(OK)	Cancel Help

Fig4-58 - Color Configuration



Bus Data Color	×
Bus Name: Bus1	
Data Condition: Data Min:	Data Max:
= 0	7
Select Color:	J
Cancel	Default Help

Fig4-59 - Bus Data Color

**Bus Name:** Display the selected Bus name.

**Data Condition:** Select the Data Condition to change the Bus data color. There are four options which are = , !=, In Range and Not In Range.

Data Min: Enter the min. data that is required by users.

**Data Max:** Enter the max. data that is required by users. The max. data can be used only when the set is In Range or Not In Range.

Select Color: Select the changed color according to the Bus condition set by users, the default is Green.

STEP 3. Click **Color Configuration** to open the Bus Data Color dialog box, and set the "Data Condition = 0" and Select Color is Orange.

Bus Data Color	×
Bus Name: Bus1	
Data Condition: Data Min:	Data Max:
= 0	F
Select Color:	
Cancel	Default Help

Fig4-60 - Set the Color for Bus1

Bus/Signal	Trigger	Filter	20 -20	-15	-10	-5	
▼ Bus1	•	•	() 0X1 ()	0X2 X 0X3	) <u>0x4</u> )	0X5 ( 0)	(6 <u>(</u> 0X7 )
• AO AO							
●A1 A1							

Fig4-61 - Before the Bus Data Color Setting

Bus/Signal	Trigger	Filter	-20	-15 -10	-5	5 10
▼ Bus1		•		<u> 0X2</u> 0X3	<u>(0X4 (0X5</u> )	( 0X6 ) 0X7 ) 0X0
• A0 A0						
● A1 A1			7		1	

Fig4-62- After the Bus Data Color Setting

Tip: Reserve the original state by the above steps.

STEP4. Activate the Latch Function



Activate the Latch Function: The default is not activated. When the Latch function is activated, the default

channel is A0, and there are three conditions for selecting, Rising Edge, Falling Edge and Either Edge; the default is Rising Edge.

Tip: The Latch function is available for the LAP-321000U-A, LAP-322000U-A, LAP-C(162000), LAP-C(321000)

and LAP-C(322000)Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U,

LAP-32128U-A, LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(32128) Modules.

Set the Latch function for one Bus. The setting of the Latch channel is A0; the analysis function adopts Rising Edge.

Bus	Color Config
<ul> <li>Activate the Latch Function</li> </ul>	A0 💌
	Rising Edge
rotocol Analyzer Setting	
Protocol Analyzer	Parameters Config
C ZEROPLUS LA 1-WIRE MODULE V1.10.00(	· · · · · · · · · · · · · · · · · · ·
ZEROPLUS LA 3-WIRE MODULE V1.04.00( ZEROPLUS LA AC97 MODULE V1.02.00(CN)	
CZEROPLUS LA ACITIMODULE VI. 02.00(CN	
CZEROPLUS LA BUS MODULE V1.00.00(CN0	
C ZEROPLUS LA CAN 2.08 MODULE V1.32.00	)(CN01)
CZEROPLUS LA CCIR656 MODULE V1.31.00	
CZEROPLUS LA Compact Flash 4.1 MODULE	
C ZEROPLUS LA CMOS IMAGE MODULE V1.00	

Fig4-63 - Activate the Latch Function

The picture of the waveform analysis:

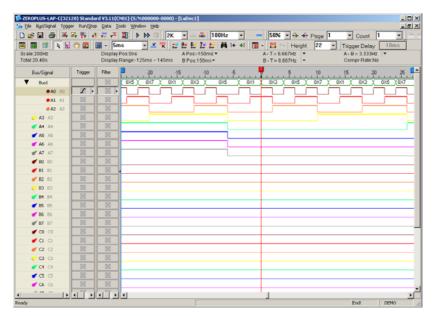


Fig4-64 - The Latch Function Displayed on the Waveform Area

Illustration: The selected channel is A0; the analysis mode is Rising Edge; it indicates that the data of the A0 is read at the Rising Edge. See the T Bar in the above figure, the data of Bus1 is 0X3.



### 4.5.2 I2C Analysis

#### **I2C Introduction**

The I2C, which stands for Inter-Integrated Circuits, is a serial synchronous half-duplex communication protocol. The I2C was first proposed by Philips Semiconductor Netherlands. This I2C protocol consists of a very simple physical interface which has only two signal channels, SDA (Serial Data) and SCL (Serial Clock). Most I2C devices consist of an independently sealed I2C chip, and this I2C chip has direct connection to both SDA and SCL. The data transmission is a byte-base (8-bit base) for every segment. Since many oscilloscopes do not allow engineers to observe timing sequence information directly from the screens of oscilloscopes, this Logic Analyzer was created to help engineers resolve timing sequence issues during their circuit development.

I2C has a multi-control Bus as its physical and firmware interfaces. This protocol analyzer is basically a signal network that may connect to one or several control units. The intention of inventing this protocol was in the application of designing television sets, which allowed the central processing unit to quicken data communications with peripheral chips and devices. The I2C interface is initiated with a SDA triggered **High** and SCL triggered **Falling Edge**. Following the initiation, there will be a set of 7 bits (or 10 bits) address space. Beyond this point, there will be Read/Write, ACK (Acknowledgement), and STOP (or HALT/HLT). The signal information packet is transmitted in bytes. If there are two or more devices trying to access the I2C protocol, whichever device has SCL at logic high will gain access priority.

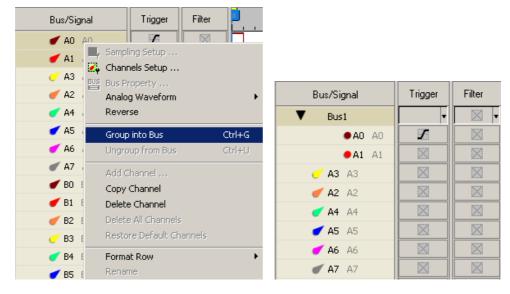
Furthermore, since I2C is a synchronous communication protocol and data transmission must be in bytes, a complete I2C signal packet must consist of **Start**, **Address**, **Read/Write**, **Data**, **ACK/NACK** and **Stop** segments. They are as following.

Start: This is the initiation of SCL and SDA (1 bit only).
Address: This identifies the device address (7 bits).
Read/Write: This is a data direction bit. 0 = Write, 1 = Read.
ACK/NACK: This is a confirmation bit following every data transmission segment.
Data: The actual signal data transmitted by byte.
Stop: This appears when SCL = High and SDA = Low (1bit only).



### 4.5.2.1 Software Basic Setup of Protocol Analyzer I2C

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- **Step2.** Set up the Falling Edge as the trigger condition on the signal which connects to the tested I2C data pin (SDA).
- Step3. Group the analytic channels into Bus1.





Step4. Select Bus 1, then, press Right Key on the mouse to list the menu. Next, click Bus Property or click Tools and the select Bus Property or click to open Bus Property dialog box.

		Bus Property	×
		Bus Setting	
		⊕ Bus	Color Config
		Activate the Latch Function	A0 👻
Bus/Signal	Trigger Filter 🧧		Rising Edge
▼ Bus1			
AC	mpling Setup	Protocol Analyzer Setting	
AC A1 BUS BUS	annels Setup	C Protocol Analyzer	Parameters Config
	alog Waveform	C ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01)	
	-	C ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01)	ㅋㅋ
🕖 A2 A2 Rev	verse	C ZEROPLUS LA AC97 MODULE V1.02.00(CN01)	
d A4 A4 Gro	oup into Bus Ctrl+G	C ZEROPLUS LA ARITHMETICAL LOGIC MODULE V1.51	.00(CN01)
🖌 AS AS Ung	group from Bus Ctrl+U	C ZEROPLUS LA BUS MODULE V1.00.00(CN01)	
		C ZEROPLUS LA CAN 2.08 MODULE V1.32.00(CN01)	
📕 🖌 A6 📕 Add	d Channel	CZEROPLUS LA CCIR656 MODULE V1.31.00(CN01)	(104)
🝼 A7 A7 Cop	py Channel	ZEROPLUS LA Compact Flash 4.1 MODULE V1.01.00( ZEROPLUS LA CMOS IMAGE MODULE V1.00.00(CN01)	
🕑 80 80 Dela	lete Channel	CEROPLOS LA CINOS IMAGE MODULE VI.00.00(CNOI	Y 1
🕑 B1 B1 Dele	lete All Channels	🔽 Use the DsDp	Find
🥑 B2 B2 Res	store Default Channels	More Protocol Analyzer	
🥑 B3 B3 Form	rmat Row 🕨		Cancel Help
d B4 B4	name		

Fig4-66 - Bus Property

Step5. For Protocol Analyzer Setting, select Protocol Analyzer. Then, choose ZEROPLUS LA I2C MODULE V2.02.00 (CN01). Next, click Parameters Configuration. The following image will appear.



ROTOCOL ANALYZER 12C	el Desite											
Pin Assignment	at   negister   Data Mode											
	Item	Name E	)ata Length									
SDA: A0	Slave Addr:	Address	7 bit									
SCL: A1	🗖 Reg Addr:	Reg Addr	8 bit									
	Data:	Data	8 bit									
Protocol Analyzer Property Write Bit  Low Level ACK Uow Level	Write Bit  Low Level  Don't stop analyzing when NACK appears											
Protocol Analyzer Color												
Start Data	Slave Addr Re		Reg Addr									
A-ACK A-NACK	D-ACK D-NA	ACK Stop	_									
	OK	Cancel	Default Help									

Fig 4-67 – Protocol Analyzer I2C Configuration dialog box

Step6. Set the I2C Configuration dialog box.

#### **Pin Assignment:**

SDA Channel: It is the Data channel, and the default is A0.

SCL Channel: It is the Clock channel, and the default is A1.

Data Mode: Set the Data Length used by the Slave Addr and the Data.

Protocol Analyzer Property:

Set the Write Bit or Read Bit to Low Level.

Set the ACK or NACK to Low Level.

**Don't stop analyzing when NACK appears**: When the option is selected, the data will be analyzed continuously when the NACK appears.

Add the Read/Write Bit for Slave Address: When the option is selected, the decoding will be displayed by way of the added Read/Write Bit for Slave Address.

Protocol Analyzer Color: Users can vary the colors of the decoded packet.

Step7. Press OK to exit the dialog box of Protocol Analyzer I2C.

Step8. Click Run to acquire I2C signal from the tested I2C circuit. Refer to Fig 4-68.

Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

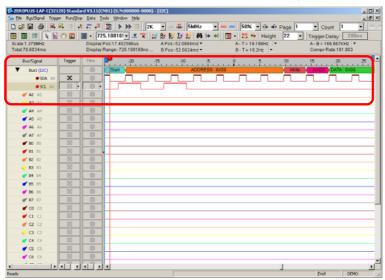


Fig 4-68 – Waveform Analysis



PROTOCOL ANALYZER I2C	×
Configuration Timing Packet Data Format Register	
Waveform Image SDA $\rightarrow$ $\leftarrow$ tsu:sro $\rightarrow$ $\leftarrow$ SCL tid:sra $\rightarrow$ $\leftarrow$ $\leftarrow$ $\leftarrow$ $\leftarrow$ tho:sra $\rightarrow$ $\leftarrow$	
Time Format Settings ✓ Activate Time Settings ✓ tHD:STA: 0.50 to: 50.00 us ✓ tSU:DAT: 0.20 to: 50.00 us	
I tHD:DAT: 0.20 to: 50.00 us II tSU:STO: 0.50 to: 50.00 us	
OK Cancel Default Help	

### 4.5.2.2 Protocol Analyzer I2C Timing Analysis

Fig 4-69 – Protocol Analyzer I2C Timing dialog box

Waveform Image: Describe the position of the set time.

**Time Format Settings**: When the Time Settings is activated, the set time will become the condition of judging decoding. For example, when you want to decode START, you should judge whether the conditions of START are satisfied firstly, and then judge whether the set time of tHD: STA is coincident with the factual waveform. If the two conditions are satisfied, the START can be decoded. Other segments decoding of the packet is the same with that of the START.



PROTOCOL ANALYZER	12C			×
Configuration Timing	Packet Data Format	Register		
ltem	Color	ltem	Color	
Slave Addr		A-NACK		
🔽 Read		D-ACK		
Vrite Vrite		D-NACK		
🔽 Data		🔽 Describe		
A-ACK		🔽 Reg Addr		
		OK	Cancel Default	Help

### 4.5.2.3 Protocol Analyzer I2C Packet Analysis

Fig4-70 - Protocol Analyzer I2C Packet dialog box

In the Packet dialog box, users can select the set item to be displayed and the color of item. It is a Bus Packet List view, which includes 4 formats, which I2C happens as follows.

Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK
1	Bus1(I2C)	-1us	50	Write	A-ACK	00	D-ACK	75	D-ACK	01	D-ACK	23	D-ACK	45	D-ACK
DATA DIADK															
Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK						
2	Bus1(i2C)	10.2064ms	50	Write	A-ACK	00	D-ACK	75	D-ACK						
Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-NACK	DESC	RIBE						
3	Bus1(i2C)	10.2982ms	50	Read	A-ACK	01	D-NACK	DATA	NACK						
Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-NACK	DESCR	RIBE		
4	Bus1(i2C)	10.3554ms	50	Read	A-ACK	23	D-ACK	45	D-ACK	67	D-NACK	DATA N	IACK		
Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK
5	Bus1(I2C)	20.477ms	50	Write	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-ACK
DA															

Fig4-71 - Protocol Analyzer I2C Packet List

Packet1: It is commonly normal data, which includes 1 "Address" and 6 "Data".
Packet2: It is commonly normal data, which includes 1 "Address" and 6 "Data".
Packet3: It is commonly normal data, which includes 1 "Address" and 14 "Data".
Packet4: It is commonly normal data, which includes 1 "Address" and 6 "Data".
Packet4: It is commonly normal data, which includes 1 "Address" and 6 "Data".

When judging the start of I2C, it is the Packet TimeStamp.

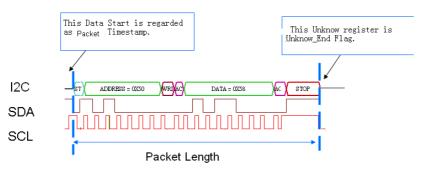


Fig4-72- Packet Length

Packet Length: From START (Start's TimeStamp) to STOP (Unknow\_End Flag TimeStamp).

Packet Idling Length: From Unknow\_End Flag TimeStamp to Start's TimeStamp.

This Unknow register is Unknow\_End Flag.

PROTOCOL ANALYZER 12					×
Configuration Timing F	acket Data Fo	rmat Register			
Ctivate					
Data:	C Binary	C Decimal	Hexadecimal	C ASCII	
Slave Addr:	🔿 Binary	C Decimal	Hexadecimal		
Reg Addr:	C Binary	C Decimal	Hexadecimal	C ASCII	
			OK Can	cel Default	Help

### 4.5.2.4 Protocol Analyzer I2C Data Format Analysis

Fig4-73- Protocol Analyzer I2C Data Format dialog box

Users can set the Data Format of the Data, Slave Addr and Reg Addr as their requirements. When selecting the option, Activate, the data formats are decided by the settings in the Protocol Analyzer; when not selecting the option, Activate, the data formats are decided by the settings in the main program.



### 4.5.3 UART Analysis

### **UART Introduction**

The UART, which stands for Universal Asynchronous Receiver/Transmitter, is a serial asynchronous protocol. The UART is often time-integrated into PC communication devices, and it usually equips an EEPROM (Electronic Erasable/Programmable Read Only Memory) for error checking proposes with other chips. There are two concepts about UART which must be understood before performing any further tasks.

The UART protocol will first translate a parallel data into serial data, for the UART requiring only one wire to transmit signals. The transmission starts at a triggered Low position, and there are 7 or 8 bits of data following afterwards. To halt a transmission, it requires a signal or multiple bits of logic '1'. Odd number bit transmission requires odd parity error checking, and even number bit transmission requires even number error checking. Following the parity check is another data translation from serial data to parallel data. UART also generates an extra signal to indicate receiving and transmitting conditions.

Furthermore, since UART is an asynchronous communication protocol and data transmission may not be in bytes, a complete UART signal Packet must consist of **Start**, **Data**, **Psrity**, **Stop**, **Baud** and **TXD** segments. They are as following:

Start: When TXD is changing from HIGH to LOW voltage (1 bit).

Data: Users must decide the size of signal Packet segment from 4 to 8bits.

Parity: This performs three types of parity checks: odd parity, even parity, and none parity.

Stop: This occurs when TXD is at high voltage. This is adjustable; this is commonly set to 1 or 2.

Baud: This is the data transmission speed according to the initial condition of START.

**TXD**: This is the transmission direction. It is MSB  $\rightarrow$  LSB by default.



### 4.5.3.1 Software Basic Setup of Protocol Analyzer UART

- **Step1.** Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1. (Tip: The Setup of the Frequency should be higher, but not too far away from the Baud Rate of the test board).
- **Step2.** Set up Either Edge as the trigger condition on the signals which are connected to the Tx pin or the Rx pin of the tested UART board.
- **Step3.** Set up the Protocol Analyzer UART dialog box. The Protocol Analyzer UART dialog box is set as the steps of I2C.

PRO	TOCOL ANALY	ZER UART						×
Co	onfiguration Pa	cket Data For	mat   F	Register				
	– Pin Assignmer	ıt						1
	Channel:	A0	•					
	– Protocol Analy	zer Property-						
	Parity Check:	None Parity	•	Data Length:	8 💌	Baud Rate:	9600 🔽 🗖 Auto	
	Stop Bit:	1	•	Percentage Sample:	70% 💌	(Min:1bps, I	Max:10Mbps)	
	Transmission Direction:	LSB->MSB	•	🔲 Data Re	verse Decoding			
	Protocol Analy	zer Color						
		Start				Data		
		Parity				Stop		
								J
					ОК	Cancel	Default Help	

Fig 4-74 – Protocol Analyzer UART Configuration dialog box

Step4. Set the UART Configuration dialog box

#### **Pin Assignment:**

UART only needs one channel to decode the signals, the default is A0.

#### **Protocol Analyzer Property:**

**Parity Check**: There are three options on the dropdown menu: None Parity, Odd Parity and Even Parity, and the default is None Parity.

Data Length: Set the Data Length in the range from 1 to 56.

**Stop Bit**: Select the Stop Bit from the three options: 1, 1.5 and 2, and it is stopped in the High Level. **Percentage Sample**: Users can select the Percentage from the options (50%, 60%, 70%, 80% and 90%) on the dropdown menu, and the default is 70%.

Transmission Direction: Set the Transmission Direction to MSB->LSB or LSB->MSB.

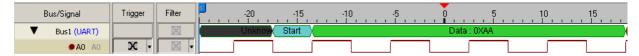
Bus/Signal	Trigger	Filter	P
Bus1 (UART)	-	•	OXAA Data : 0XAA 📕 Data : 0XAA Data : 0X55 )
• A0 A0			
🝼 A1 A1			
🥑 A2 A2			
Bus/Signal	Trigger	Filter	₽ -20 <del>^ </del> -10 -5 ₽
Bus/Signal Bus1 (UART)	Trigger	Filter	-20 -5 -10 -5
Bus1 (UART)		-	

Fig 4-75 – Data Waveforms MSB->LSB and LSB->MSB

Baud Rate: The dropdown menu has options as below: 110, 300, 600, 1200, 2400, 4800, 9600, 19200,

38400, 57600, 115200, 230400, 460800 and 921600. Users can select the desired value from the menu. At the same time, The **Auto** can be selected to calculate the Baud Rate automatically (If the Auto is selected, the Baud Rate will be calculated and displayed on the Configuration dialog box automatically.).

Data Reverse Decoding: When the option is selected, the data will be decoded in reverse.





Bus/Signal	Trigger	Filter	<b>5</b> 	-20	-15	-10	-5	0	5	10	15	20	25
Bus1 (UART)		$\square$	Unknow	(Start )			Data : (	IXAA		Data	: OXAA		
• A0 A0	х -	-											

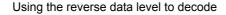


Fig 4-76 - Without/With the Reverse Data Level for Decoding

#### Protocol Analyzer Color:

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

Users can vary the colors of the decoded packet.

Step5. Press OK to exit the dialog box of Protocol Analyzer UART.

Step6. Click Run to acquire the UART signal from the tested UART circuit. Refer to Fig 4-77.

Tip: Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

I 😂 🖬 🎒 🙀 I 📰 💕 N 🕅 cale:24.355KHz otal:335.18149ms		Display	.05969; Pos:27.0	' <b>। ▼ .≝ ^</b> 994ms		AF B∦ T∦ A Pos:-167.	100MHz	• •i   🔀	T = 5	▼ +	Page	▼ Trig	Count ger Dela 9 = 3.3331 npr-Rate:	y 10n MHz  ▼	s é
Bus/Signal	Trigger	Filter	B	-20	-15				0	5	. 10	15		20	25
Bus1 (UART)			Start			Data : 0X37		St	art		Data : 0	IXC2		Stop	Unkne
•A0 A0	X				4		1							-	
A1 A1	-		۲		L		L							L	
A3 A3		$\overline{\otimes}$													
A4 A4															
✓ A5 A5															
🝼 A6 A6		$\otimes$													
✓ A7 A7		$\otimes$													
<b># 80</b> 80															
🥑 B1 B1															
🥑 B2 B2		$\square$													
🥑 B3 B3															
🥑 B4 B4															
<b>6 B5</b> B5			<u> </u>												
✓ B6 B6															
✓ B7 B7 ✓ C0 C0															
<b>G</b> G G															
C4 C4		$\overline{\otimes}$													
<b>C5</b> C5		$\otimes$													
		$\overline{\otimes}$													

Fig 4-77 – Waveform Analysis



PROTOCOL A	NALYZER UART					×
Configuration	n Packet Data	Format Register	1			
	Item	Color	I	ltem	Color	
	🔽 Data		l	Parity		
	🔽 Describe					
_						_
	Packet Idle(1	ime):	5ms	(Min:10ns, Max:10s)		
			← Time →			
	- Data:	OXC2	UNKNOW D	ata: OX62	UNKNOW	
						-
			ОК	Cancel	Default	Help
					Dicidait	Trop

### 4.5.3.2 Protocol Analyzer UART Packet Analysis

Fig4-78 - Protocol Analyzer UART Packet dialog box

Data: List Data field captured by Bus in the packet display.

Parity: Display parity check in packet.

Describe: Error description to any field (format or data bit).

**Packet Idle (Time):** When the check box is selected, the default value is 5ms. Specifically, when the Packet Idle (Time) is activated, the packet will be divided again according to the Packet Idle (Time). If the Time Length between the previous packet and the next packet is more than 5ms, the two packets will still be divided, or the two packets will be merged into one packet.

It is a Bus Packet List view, which includes 4 formats, which UART happens below. PARITY clews whether users start PARITY or not.

JS Packet Li Setting	ist Refresh Export	Synch Par	ameter			_	
Packet #	Name	TimeStamp	Data	Parit	у		
1	Bus1(UART)	-21927	B6	Even Parity			
Packet #	Name	TimeStamp	Data	Parity		DESCRIBE	
2	Bus1(UART)	81164	6C	Error-0	Parit	y Error,should Low	7
Packet #	Name	TimeStamp	Data	Parit	у		
3	Bus1(UART)	184247	D9	Even Parit	ty		
Packet #	Name	TimeStamp	Data	Parity			
4	Bus1(UART)	307617	EC	Even Parit	ty		



Packet1: It is commonly normal Data, which includes 1 "Data" and 1 "Parity"; its parity is Even Parity.

Packet2: It is the state of Parity Error; the DESCRIBE is "Parity Error, should Low ".

Note: Because the Even Parity and the Odd are impossible to present to the same Bus, so we only take the Even Parity for an example here.

Packet3: It is commonly normal Data, which includes 1 "Data" and 1 "Parity"; its parity is Even Parity.



**Packet4:** It is commonly normal Data, which includes 1 "Data" and 1 "Parity"; its parity is Even Parity. Packet Length: When judging to the start of UART, it is the packet TimeStamp.

#### State 1: Having Stop:

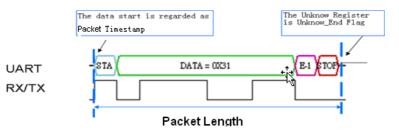
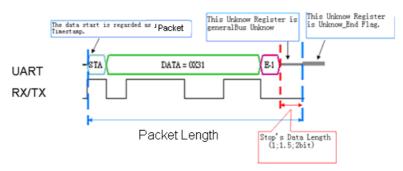


Fig4-80 - Packet Length

#### State 2: No Stop:





If the STOP falls short of condition, it isn't noted down in UART.

Packet Length: From START (Start's TimeStamp) to STOP (Unknow\_End Flag TimeStamp)

Packet Idling Length: Unknow\_ End Flag TimeStamp to START TimeStamp.



#### 4.5.4 **SPI** Analysis

#### **SPI Introduction**

SPI (Synchronous Peripheral Interface) is a parallel synchronous full duplex protocol with a Bus-like physical interface. This protocol was first developed by Motorola and was generally used for EEPROM, ADC, FRAM, and display device drivers which are equipped with low data transmission speed. The SPI data transmission is synchronous in both receiving and transmitting directions. Although Motorola initially did not define the clocking impulse, it is commonly seen that the clocking impulse is according to the master processor. In practice, there are two clocking impulses: CPOL (Clock Polarity) and CPHA (Clock Phase). The configuration of both CPOL and CPHA decides the sampling rate. When the SPI must transmit serial data, it initiates the highest bit.

Since SPI is a synchronous communication protocol and data transmission may not be in bytes, a complete SPI signal Packet must consist of SCK, MOSI, MISO, and SS segments with CPHA and CPOL. They are as following.

SCK: Serial Clock Line (SCL).

MOSI: Master data output, Slave data input (MOSI stands for Master-Out-Slave-In).

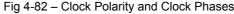
MISO: Master data input, Slave data output (MISO stands for Master-In-Slave-Out).

SS: SS stands for Signal Selector of the master device which is to select signals for the Slave devices.

CPHA: The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats.

CPOL: The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock.

The state state state that state the	The dold are driven and somerca
J J J J J J	JOJOJOL
Clock Polarity = 0 where rising edges happen Clock Phase = 0 where wave cycle start	Clock Polarity = 0 where rising edges happen Clock Phase = 1 where wave cycle end
The data are driven and sampled	Rue duta are driven and samulard
Clock Polarity = 1 where rising edges happen Clock Phase = 0 where wave cycle start	Clock Polarity = 1 where rising edges happen Clock Phase =1 where wave cycle end
Fig 4-82 – Clock Pol	arity and Clock Phases





### 4.5.4.1 Software Basic Setup of Protocol Analyzer SPI

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Set up the Falling Edge on the signal of SS which connected to the Signal Selector (SS) pin of the SPI tested board.
- Step3. Set up the Protocol Analyzer SPI dialog box, the Protocol Analyzer SPI dialog box is set as the steps of I2C.

PROTOCOL ANALYZER SPI	
Configuration Packet Data Format Register	
Pin Assignment       SCLK:       DATA:       A1       Protocol Analyzer Property       Mode:       CPHA=0,CPOL=0       Transmission       Direction:	SS Pin Assignment SS Channel SS Channel: A0 SS Setting: Uitual SS Idling Time: 20ns (Mim:20ns: Max1.3111ms)
Data Length:  8 bit Fill"0" at the LSB when the bit count is not enough.	🔽 Don't care data bit
Protocol Analyzer Color	
Data	
OK	Cancel Default Help

Fig 4-83 – Protocol Analyzer SPI Configuration dialog box

Step4. Set the SPI Configuration dialog box

#### **Pin Assignment:**

**SCLK:** It is the Clock channel, and the default is A0. **DATA:** It is the Data channel, and the default is A2.

#### **Protocol Analyzer Property:**

#### Mode:

There are six modes for selecting, which are CPHA=0,CPOL=0; CPHA=1,CPOL=1; CPHA=1, CPOL=0; CPHA=0, CPOL=1; Rising and Falling. **Transmission Direction:** Set the Transmission Direction to MSB->LSB or LSB->MSB. **Data Length:** Set the Data Length in the range from 1 to 56, and the default is 8.

**Fill "0" at the LSB when the bit count is not enough:** For example, the value of Data is "1001111", there is only 7 Bits. When the value of Data is set to 8 Bits, the displayed value should be 10011110.

#### SS Pin Assignment:

**SS Channel:** Select the channel for the SS, the default is A1.

**SS Setting:** Set the Judgment Level of the SS Channel to Low or High.

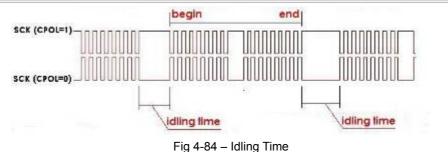
Virtual SS: When the SS Channel is not activated, the Virtual SS will be activated. The Idling Time of the

Virtual SS should be set as an auxiliary condition to decode.

Type the idling time of the SCLK signal on the tested SPI circuit. The idling time is defined as the idling

time as shown in Fig 4-86.





Protocol Analyzer Color: Users can vary the colors of the decoded packet.

Step5. Click OK to exit the dialog box of Protocol Analyzer SPI.

Step6. Click Run to acquire the SPI signal from the tested SPI circuit. Refer to the Fig 4-87.

Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

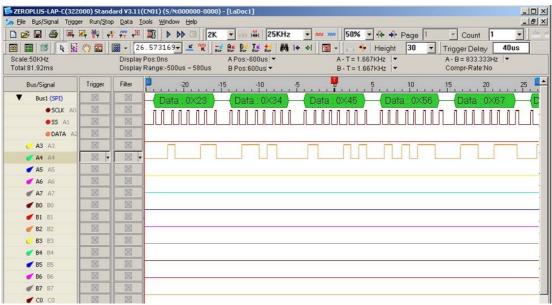


Fig 4-85 – SPI Signal



### 4.5.4.2 Protocol Analyzer SPI Packet Analysis

Ρ	ROTOCOL ANALYZER S	5PI	×
	Configuration Packet	Data Format Register	
	Item	Color	
	🔽 Data		
		OK Cancel Default Help	

Fig4-86 - Protocol Analyzer SPI Packet dialog box

DATA: List Data field captured by Bus in the packet display.

#### BUS Packet List:

BUS Packet L	US Packet List											×	
Setting	Setting Refresh Export Synch Parameter												
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data		
1	Bus1(SPI)	57	12	23	34	45	56	67	78	89	9A		
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data		
2	Bus1(SPI)	415	12	23	34	45	56	67	78	89	9A		
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data					
3	Bus1(SPI)	774	12	23	34	44	AC	CE	]				
													<b>_</b>
1													

Fig4-87 - Protocol Analyzer SPI Packet List

Packet Length and Packet Idling Length

1. SS channel is activated

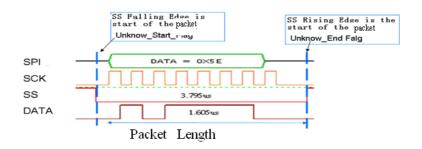


Fig4-88 - Packet Length

Packet Length: From Unknow\_Start\_Flag TimeStamp to Unknow\_ End Flag TimeStamp

Packet Idling Length: From Unknow\_End Flag TimeStamp to Unknow\_Start\_Flag TimeStamp

2. SS channel is not activated.



Virtual SS is activated 1: Data needs 8-bit; the Idling Time is set as 3us.

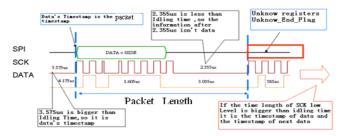
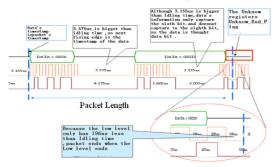


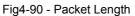
Fig4-89 - Packet Length

Packet Length: From Unknow\_Start\_Flag TimeStamp to Unknow\_ End Flag TimeStamp

Packet Idling Length: From Unknow\_End Flag TimeStamp to Unknow\_Start\_Flag TimeStamp

Virtual SS is activated 2: Data needs 8-bit; the Idling Time is set as 3us. Don't care data bit is not activated.





Packet Length: From Unknow\_Start\_Flag TimeStamp to Unknow\_End Flag TimeStamp

Packet Idling Length: From Unknow\_End Flag TimeStamp to Unknow\_Start\_Flag TimeStamp

Virtual SS is activated 3: Data needs 8-bit; the Idling Time is set as 3us. Don't care data bit is activated.

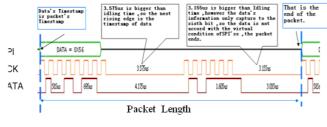


Fig4-91 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data

Packet Idling Length : It is 0.

The End dot is Unknown.

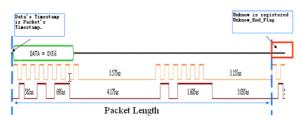


Fig4-92 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data Packet Idling Length: It is 0.



### 4.5.5 1-WIRE Analysis

### Preface

To increase the Protocol Analyzer feature in order to analyze the Protocol Analyzer 1-WIRE transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Bus. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer 1-WIRE dialog box.

### **1-WIRE Introduction**

1. Brief Introduction

#### Features

1-WIRE is a non-synchronic half-duplex serial transmission, which requires only one OWIO to transmit data. The typical 1-WIRE transmission structure is illustrated in Figure 4-95. During the 1-WIRE transmission, the OWIO can be used to transmit data and supply power to all devices connected to the 1-WIRE. OWIO will link to a 4.7K Ohm Pull-High electric resistance which is linked to the power supply (3V-5.5V). The transmission speed for 1-WIRE can be divided into two types, standard and high speed. Every 1-WIRE has a unique 64-bit code for the device to recognize. Therefore, the maximum number of link devices is 1.8; almost unlimited.

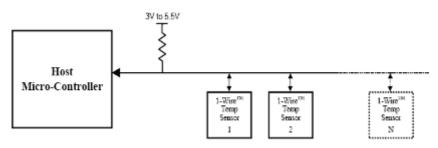


Fig4-93 - Applications

#### Applications

1-WIRE is commonly applied to the EEPROM and to certain sensor interfaces.

#### 2. Protocol Analyzer Signal Specifications

Parameter	Value					
Name of Protocol Analyzer	1-WIRE					
Required No. of Channels	1					
Signal Frequency	Not fixed, around 10K					
Appropriate Sampling Rate	1MHz					
Same Data Time Per Bit	⊡Yes ∎No					
Name of Syn. Signals	OWIO					
Data Verification Point	30 us after the falling edge signals					

#### 3. Protocol Analyzer IO Description

Name	Function
OWIO	The only I/O transmits Reset signals and data.

#### 4. Protocol Analyzer Electrical Specifications

Parameter	Min.	Тур.	Max.	Unit	Note
High-count Voltage	2.8		5.2	V	Every IC varies according to the Pull-High voltage.
Low-count Voltage		0		V	



### **Protocol Analyzer 1-WIRE Format Description**

Two speed types of 1-WIRE: Standard: 1MHz (1us) High: 5MHz (0.2us) Four types of 1-WIRE Signals:

1. Reset:

Every communications period starts with Reset signal. Master will send a Reset Pulse so that all the Slave devices on the 1-WIRE Protocol Analyzer enter into recognition status. When one or many Slaves receive Reset Pulse, a Presence Pulse signal will be sent back from Slave, indicating receipt of the signal.

- 2. Write 0: Send a "0" bit to Slave (Write 1 time slot).
- 3. Write 1: Send a "1" bit to Slave (Write 1 time slot).
- 4. Read Data:

"Read data sequences" resembles "Write time slot." However, when Master releases BUS and reads data from Slave devices, Master creates samples from BUS status. In this way, Master can read any 0 or 1 bit from Slave devices.

Four signal types are described respectively in the following:

- 1. Reset:
  - (1) When Master starts communicating with Slave, Master first sends a low-count Reset Pulse (TX)
    - of *L<sub>RSTL</sub>* (Standard speed: 480us; High Speed: 48us) for a period of time.

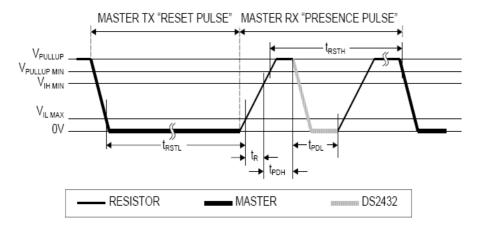


Fig4-94 - Master TX Reset Pulse and Master RX Presence Pulse

- (2) Then, Master releases Protocol Analyzer and enters the RX mode. Through high- pull resistor,1-WIRE Protocol Analyzer is pulled back to the high status.
- (3) Then, Master detects a rising edge from the Data Line when every slave will wait for a period of time ( $t_{PDH}^{PDH}$ ) (standard speed: 15-60us; high speed: 2-6us) and send back a Presence Pulse to Master ( $t_{PDL}^{PDL}$ )(standard speed:60-240us; high speed: 8-24us).
- (4) Finally, the 1-WIRE Protocol Analyzer will be pulled back to the high status through the resistor.
- (5) Meanwhile, Master can detect any online Slave.
- (6) From Fig4-95, the low count Reset Pulse and Presence Pulse signals can be clearly seen.



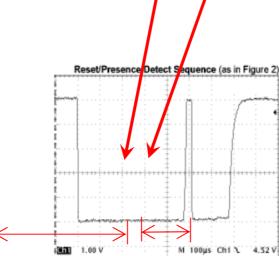


Figure 2a. You can clearly see the negative going reset and the presence pulse

#### Fig4-95 - Reset/Presence Detect Sequence

- 2. Write Data:
  - (1) To initialize Write Data, Master will convert the Data Line from the high logic to the low.
  - (2) There are two types of Write time slot: Write 1 time slot and Write 0 time slot.
  - (3) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.
  - (4) When the I/O line goes down, Slave devices create samples from 15-60 us.
    - A. Write 0: If the sampling is low, 0 is generated as in Fig4-98:



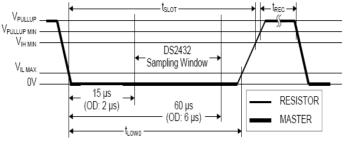


Fig4-96 - Write-zero Time Slot

B. Write 1: If the sampling is high, 1 is generated (Note: Read 1 is of a similar waveform pattern) as in Fig4-99:

Write-one Time Slot

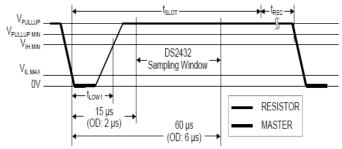


Fig4-97 - Wrote-one Time Slot



#### 3. Read Data:

- (1) When Slave reads data, Master will generate a Read time slot.
- (2) To initialize Read Data, Master has to convert Data line from the high logic to the low.
- (3) Data line must be kept as low as 1us.
- (4) The Output Data of Slave must be 14us at most.
- (5) To read from 15us where Read slot starts, Master must stop driving I/O.
  - Read-data Time Slot

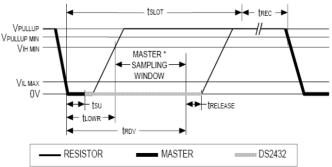


Fig4-98 - Read-data Time Slot

- (6) When Read Time Slot ends, I/O Pin will be pulled back to the high count through the external resistor.
- (7) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.
- 4. Typical 1-WIRE Conversation model can be summarized as below:

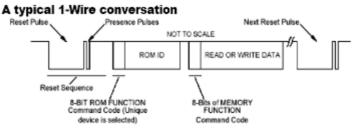


Diagram 1 typical 1-Wire communication sequence.

Fig4-99 - A Typical 1-WIRE Conversion

- (1) Master keeps Protocol Analyzer at low signal (standard speed: 480us; high speed: 48us) as the Reset Pulse.
- (2) Then, Master releases Protocol Analyzer and locates a Presence Pulse responded by any online Slave.
- (3) The above two points are Reset Pulse and Presence Pulse, which can be put together as a Reset Sequence.
- (4) If Presence Pulse is detected, the slave location will enable Master to access Slave using the Write 0 or Write 1 Sequence.



- 5. 1-WIRE Serial Number:
  - (1) Every 1-WIRE Slave has a unique laser memory.
  - (2) The serial number is 64bits.
  - (3) The serial numbers are 8bytes in total, located in three individual, which are illustrated as below:

MSB		64 <b>-</b> bi	t 'Registration' ROM nur	nber		LSB
8-bit C	CRC		48-bit Serial Number		8-bit Fan	nily Code
MSB	LSB	MSB		LSB	MSB	LSB

- (4) Starting from LSB, the first byte is for family code, which is used to identify product categories.
- (5) Next, the 48bits is the only address for storage.
- (6) The last byte, MSB is used to store CRC.



PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us
(Min:1bit,Max:32bit)	(Min:1,Max:120)
OK	Cancel Default Help

## 4.5.5.1 Software Basic Setup of Protocol Analyzer 1-WIRE

Fig4-100 - Protocol Analyzer 1-WIRE Configuration dialog box

Set the 1-WIRE Configuration dialog box.

#### Pin Assignment:

1-WIRE only needs one channel to decode the signals, and the default is A0.

#### Connect Speed:

The Connect Speed can be set to Standard(1 us) or High(0.2 us).

#### Transmission Direction:

The Transmission Direction can be set to MSB->LSB or LSB->MSB.

MSB->LSB: From High Level to Low Level.

LSB->MSB: From Low Level to High Level.

#### Data Length:

The Data Length can be set in the range from 1 to 32-bit, and the default is 8-bit.

#### Sampling Position:

The Sampling Position can be set in the range from 1 to 120us, and the default is 30us.

#### Protocol Analyzer Color:

Users can vary the colors of the decoded packet.



## **User Interface Instructions**

Set up the Protocol Analyzer 1-WIRE dialog box which is set as the steps of I2C.

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
0W10: A0	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us
(Min:1bit,Max:32bit)	(Min:1,Max:120)
OK	Cancel Default Help

Fig4-101 - Protocol Analyzer 1-WIRE Configuration dialog box

#### STEP 1. Select Channel

1-WIRE has only one OWIO. Select the channel that it is to link the OWIO.

PROTOCOL ANALYZER 1-WIRE				×
Configuration Packet Data Fo	ormat Register			1
Pin Assignment		– Protocol Analyzer	Color	
0W10: 🗚	Ē	Reset Pulse		
Protocol Analyzer Property		Presence Pulse	,	
Connect Speed: Standard	(1 us) 💌	Data		
Transmission MSB->Ls Direction:	iB 💌	- Sampling Position	1	
Data Length: 8	bit	30 us		··
(Min:1bit	,Max:32bit)	(Min:1,Max:120	)	
	OK	Cancel	Default	Help

Fig4-102 - Protocol Analyzer 1-WIRE Channel Setup



#### STEP 2. Set the Connect Speed

1-WIRE has two modes: Standard(1 us) and High(0.2 us). The speed setup according to the specifications of the object to be tested and the default mode is standard.

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
0W10:	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data 🗾 😳
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us 4005
(Min:1bit,Max:32bit)	(Min:1,Max:120)
ОК	Cancel Default Help

Fig4-103 - Protocol Analyzer 1-WIRE Connect Speed Setup

#### STEP 3. Set the Transmission Direction

Set the Transmission Direction as either MSB -> LSB or LSB -> MSB.

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	1
Pin Assignment	Protocol Analyzer Color
0W10: A0 💌	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data
Direction:	Sampling Position
Data Length: 8 bit	30 us 1005
(Min:1bit,Max:32bit)	(Min:1,Max:120)
ОК	Cancel Default Help

Fig4-104 - Protocol Analyzer 1-WIRE Transmission Direction Setup

### STEP 4. Set the Sampling Position

Users can slightly adjust the sampling position of 1-WIRE. This feature is applicable when the signal cannot be decoded. The default value is 30us.



PROTOCOL ANALYZER 1-W	IRE		X
Configuration Packet Da	ata Format   Register		
Pin Assignment		Protocol Analyzer Color	
0WI0: A0	<u> </u>	Reset Pulse	
Protocol Analyzer Proper	ty	Presence Pulse	
Connect Speed: Star	ndard(1 us) 💌	Data	
Transmission MSI Direction:	B->LSB ▼	Sampling Position	
Data Length: 8	bit	30 us 3000	
(Mir	n:1bit,Max:32bit)	(Min:1,Max:120)	
	OK	Cancel Defau	ult Help

Fig4-105 - Protocol Analyzer 1-WIRE Sampling Position Setup

### STEP 5. Set the Data Length

This function decides how many bits of data can be combined as one set of figures. The default is 8 bits, and the maximum is 32bits.

PROTOCOL ANALYZER 1-WIRE	X
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
0WI0: A0	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data 🗾 😳
Transmission MSB->LSB	Sampling Position
Data Length: 8 Dit	30 us
(Min:1bit,Max:32bit)	(Min:1,Max:120)
ОК	Cancel Default Help

Fig4-106 - Protocol Analyzer 1-WIRE Data Length Setup



ROTOCOL A	NALYZER 1-WIR	E			3
Configuratio	n Packet Data	Format Register			
	Item	Color			
	🔽 Data				
	🔽 Describe				
		OK	Cancel	Default	Help

## 4.5.5.2 Protocol Analyzer 1-WIRE Packet Analysis

Fig4-107- Protocol Analyzer 1-WIRE Packet dialog box

That is the new View; the below View includes several formats that 1-WIRE can happen; it describes Data number and their positions.

3US Packet L	ist																			
Setting	Refresh Export	Synch Parame	eter																	
Packet #	Name	TimeStamp	1	_							Data									
1	Bus1(1-WIRE)		33	96	30	96	03	90	02	48	B7	FF	FF	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp	Í								Data	1								
2	Bus1(1-WIRE)	8065053	33	96	30	96	07	90	00	48	F7	FF	FF	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp									Data	1								
3	Bus1(1-WIRE)	12096936	33	96	30	96	03	90	02	48	8F	FF	FF	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp									Data	1								
4	Bus1(1-WIRE)	16129232	33	96	30	96	03	90	02	48	8F	FF	FF	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp									Data	1								
5	Bus1(1-WIRE)	20161527	33	96	30	96	07	90	01	48	2F	FF	FF	FF	FF	FF	FF	04	00	

Fig4-108 - Protocol Analyzer 1-WIRE Packet List

Packet 1: It is commonly normal Data, which includes 1 "Data".
Packet 2: It is commonly normal Data, which includes 1 "Data".
Packet 3: It is commonly normal Data, which includes 1 "Data".
Packet 4: It is commonly normal Data, which includes 1 "Data".
Packet 5: It is commonly normal Data, which includes 1 "Data".
Packet 5: It is commonly normal Data, which includes 1 "Data".



## 4.5.6 HDQ Analysis

### Preface

Increase the Protocol Analyzer feature to analyze the Protocol Analyzer HDQ transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Protocol Analyzer. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer HDQ dialog box.

## **HDQ Introduction**

### **1. Brief Introduction**

### Features

Protocol Analyzer HDQ is a non-synchronic half-duplex serial transmission, which requires only one HDQ and uses a quasi-PWM (Pulse Width Modulation) to verify the serial data.

### Applications

HDQ is commonly applied to the display interface for battery management.

### 2. Protocol Analyzer Signal Specifications

Parameter	Value						
Name of Protocol Analyzer	HDQ						
Required No. of Channels	1						
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz						
Appropriate Sampling Rate	100MHz						
Same Data Time Per Bit	□Yes ■No						
Name of Syn. Signals	HDQ						
Data Verification Point	Low signals > 190us converts to High signals > 40us						

### 3. Protocol Analyzer IO Description

Name	Function
HDQ	The sole I/O transmits Host and BQ-HDQ status and data.

#### 4. Protocol Analyzer Electrical Specifications

Parameter	Min.	Туре	Max.	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

## **Protocol Analyzer HDQ Format Description**

The format changes according to the pulse width, so the display must refer to the defined pulse width. Protocol Analyzer HDQ is made up of 16 bits signals. Firstly, after the period of status signals, a device will be installed for the 7 bits address through the Host so that 1-bit signals can be read or written. After a response time of high signals, data will be exported in 8 bits format with the data and location content from LSB to MSB. The following is the Host to BQ-HDQ analysis.



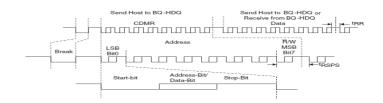


Fig4-109 - Host to BQ-HDQ Analysis

# **Protocol Analyzer Format**

### Break

This is the initial bit for the Protocol Analyzer HDQ: after Low signal lasting a period of t (B), it is then converted to a High signal lasting a period of t(BR). The length of Low signal is no less than 190us whereas the High signal is no less than 40us.

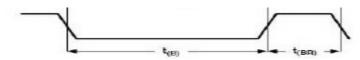


Fig4-110 - Pulse from Low to High

### Address

The Address comprises 7 bits. The initial Low signal lasts a period of t(HW1) and if the write-0 status continues through the end of the t(HW0) period, the signal will convert to High and last throughout the period of t(CYCH), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(HW1) period of time, the signal will convert to High and last throughout the period of t(CYCH), which is of 1 bit and no less than 190 us. The t(HW1) range is from 0.5us to 17us and no more than 50us. The t(HW0) range is from 86us to 100us and no more than 145us.

### Read/Write

Read/Write is 1 bit. 0 and 1 are displayed in the same way as the above description.

### T (RSPS)

The High signal lasts a period of 190us-320us. The following 8-bit data is Send Host to BQ-HDQ or Receive from BQ-HDQ Data.

### Data

Made up by 8 bits, and it is Send Host to BQ-HDQ or Receive from BQ-HDQ Data. It operates in the same way as in 2.2 and the data is from LSB to MSB.

#### **BQ-HDQ To Host**

If the data transmission is read by BQ-HDQ To Host, the initial Low signal lasts a period of t(DW1) and if the write-0 status continues through to the end of the t(DW1) period, the signal will convert to high and last throughout the period of t(CYCD), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(DW1) period of time, the signal will rise and last throughout the period of t(CYCD), which is of 1 bit and ranges from 190us to 260us. The t(DW1) ranges from 32us to 50us and no more than 50us. The t(DW0) ranges from 80us to 145us.

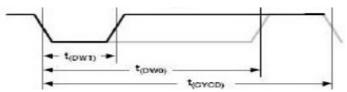


Fig4-111 - Signal from BQ-HDQ to Host



# 4.5.6.1 Software Basic Setup of Protocol Analyzer HDQ

PROTOCOL ANALY	zer hdq							×
Configuration Pa	icket Data For	mat	Register					
Pin Assignment Channel:	A0 🔽							
- Time Settings(u	.e.							
Break:	190	to	1000000	Recovery:	40	to	1000000	
Host 1:	0	to	70	Device 1:	0	to	70	
Host 0:	80	to	180	Device 0:	80	to	180	
Host Bit:	190	to	260	Device Bit:	190	to	260	
Response:	190	to	320	Remark:1000	1000 is infinite			
Protocol Analyz	zer Color							
Break	Recover	y	Address	Read	Write		Data	
	·			•				
				ок	Cancel	Defa	ult Help	

Fig4-112 - Protocol Analyzer HDQ Configuration dialog box

Set the HDQ Configuration dialog box.

#### **Pin Assignment:**

HDQ has only one signal channel, therefore it only specifies the name of the channel and marks the selected channel.

Protocol Analyzer Name: Display the name of the selected Bus.

Channel: Preset as A0.

Timing Settings(us):

Set the time for Break, Address, Read, Write, Data and Recovery.

Protocol Analyzer Color: Users can vary the colors of the decoded packet.



# **Operating Instructions**

Open the LA operation interface.

	_ 8 ×
Image: Scale:25KHz       Display Pos:0ns       A Pos:-600us   *       A - T = 1.667KHz       Y       A - B = 833.333         Total 31.92ms       Display Pos:0ns       A Pos:-600us   *       B - T = 1.667KHz       Y       A - B = 833.333         Bux/Signal       Trigger       Filer       -20       -3       -10       5       7       5       10       -10       2       20         Image: All All       All All	
Scale:25KHz         Display Pos:0ns         A Pos:-600us   ✓         A - T = 1.667KHz         ✓         A - B = 833.333+           Total:81.92ms         Display Range-1ms ~ 1.08ms         B Pos:600us   ✓         B - T = 1.667KHz         ✓         A - B = 833.333+           Buz/Signal         Trigger         Filer         ✓         -20         -3         10         5         5         10         -20         -20         -3         10         -20         -3         20         -20         -20         -3         10         -5         7         5         10         -20         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         20         -3         10         -20         -3         10         -20         -3         20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20         -3         10         -20	<u>▼</u> _4 :
Total 81.92ms         Display Range: 1ms ~ 1.08ms         B POS:600us] +         B - T = 1.667kHz         •         Compr-Rate.No           Buc/Signal         Trigger         Filter         -20         -3         10         -5         5         10         -75         20           A 0         A0	40us
But/Signal         Trigger         Filer         -20         -10         -5         T         5         10         -20	z 💌
Bur/Signal         Tigger         Filter         P20         75         -10         -5         T         5         10         13         20 <ul></ul>	
A1     A1       A2     A2       A3     A3       A4     A4       A5     A5       A6     A6	25 -
A2     A2       A3     A3       A4     A4       A5     A5       A6     A6	
A3         A3         A3           A4         A4         A3         A3           A5         A5         A3         A3           A6         A6         A3         A3	
A4         A4         A4           A5         A5         A5           A6         A6         A4	
AS         AS           A6         A6	
<b>A6</b> A6	
<b>67</b> B7	
	•
Ready End	DEMO

Fig4-113 - Operation Interface

Sample the HDQ signal or open the sampled waveform.

La :2. 01234as:           La :2. 10234as:           La :1. 107. 09500al           Pax/Si gnal           A 0. A0           A 1. A1           A 2. A2           A 3. A3           A 4. A1           A 5. A5           A 6. A6           A 7. A7           B 18 18           B 2. 82           B 3. 83           B 8. 83           B 8. 84	Filter	nge:-50.3085ms ~ 5 B	Pes:17.102224ms   ♥ Pes:18.91144ms   ♥ ims =70.1234ms =10. 884ms	B - T 0517ms 05s 13.5 14 14 14 14 14 14 14 14 14 14	= 17.102224ms = 16.91144ms 348ms 348ms 67.695ms 67.695ms 67.695ms 67.695ms 67.695ms		- B = 190,76425 ompz-Rate:255.85 1851ms 40,24680 133,5287	32 ns 50.30
A A         X           A I         Image: Constraint of the state o				13.5 10 10 10	348ms 67.695ms 67.695ms 67.695ms			
A1     A1       A2     A2       A3     A3       A4     A4       A5     A5       A6     A6       A7     A7       B0     B0       B1     B1       E2     B2       B3     A3		83.	884ms	10 10 10 10	67.695ms 67.695ms 67.695ms	13.442ms	13. 528r	ns
A2     A2       A3     A3       A4     A4       A5     A5       A6     A6       A7     A7       B0     B0       B1     B1       E2     B2       B3     S3				10	67.695ms 67.695ms			
A3     A3       A4     A4       A5     A5       A6     A6       A7     A7       B0     B0       B1     B1       B2     B2       B3     B3				10	67.695ms			
A4         A4           A5         A5           A6         A6           A7         A7           B0         B0           B1         B1           B2         B2           B3         B3				10				
AS         AS           AA         AA           AA         AA           AA         AA           AA         AA           AA         AA           BA         AA           BB         BA					67.695ms			
	$\otimes$			10				
A7         A7           B0         B0           B1         B1           B2         B2           B3         B3					67.695ms			
B0         B0           B1         B1           B2         B2           B3         B3				16	67.695ms			
B1         B1           B2         B2           B3         B3	$\otimes$ .			10	67.695ms			
<ul> <li>✓ B2 B2</li> <li>✓ B3 B3</li> </ul>	$\otimes$			10	67.695ms			
✓ B3 B3	$\otimes$				67.695ms			
KaN .	$\otimes$			16	67.695ms			
✓ B4 B4	8				67.695ms			
	$\otimes$				67.695ms			
✓ BS B5	8				67.695ms			
	8				67.695ms			
✓ B7 B7					67.695ms			
					67.695ms			
					67.605			

Fig4-114 - HDQ Waveform

**孕龍科技股份有限公司** Zeroplus Technology Co., Ltd.

Arrange the signal channels into Bus.

<u>F</u> ile B <u>u</u> s/Signal	T <u>r</u> igger Ru	n/Stop Data To	ols Mindow Help		
😂 🖬 🎒 🍬	🔀 🕅 🖗	👯 📲 🋐	▶ ▶▶ □ 128K ▼ ₩4 ₩1 200MHz ▼ #	₩	1 - Count 1 -
I 💷 🤔 📐 🖁	i 🖑 🛍 📗	🐹 🖌 2.01234		🕓 🛛 🔛 🔤 😽 Height 🛛 30	▼ Trigger Delay 5ns
cale:2.01234ms otal:167.69509ms		Display Pos:On Display Rongo	ns A Pos:17.102224ms V :-50.3085ms ~ 5 B Pos:16.91144ms V	A - T = 17.102224ms   ▼ B - T = 16.91144ms   ▼	A - B = 190.784252us   ▼ Compr-Rate:255.882
			. 30. 303313 3 B 105, 10, 31144iis 🗸		
Bus/Signal	Trigger	Filter	-40.2468ms -30.1851ms -20.1234ms -10.0617ms	0hs 10.0617ms 20.1234	ms 30.1851ms 40.2468ms 50.3085
🖌 A0 A0	pling Setup		83.884ms	13.348ms 📕 13.4	42ms 13.528ms
🖌 Al A 🔀 Cha				167.695ms	
🕖 A2 A 🗒 Bus	Property .			167.695ms	
	log Wavefor erse	m		167. 695ms	
🗹 🗛 🗚 Gro	up into Bus	Ctrl:	+G		
Ung	roup from B		+U	167.695ms	
🖌 A5 A 📈 Add	Channel			167.695ms	
	y Channel			167.695ms	
A7 A	ete Channel ete All Cha			167.695ms	
	tore Defaul			167.695ms	
🕑 B1 B For	mat Row		•	167.695ms	
B2 B2	ame	NA 11			
-				167.695ms	
🥑 <b>B3</b> B3		$\otimes$		167.695ms	
🥑 <b>B4</b> B4		$\otimes$		167.695ms	
🥑 B5 B5		$\otimes$		167.695ms	
🍼 B6 B6		$\otimes$		167.695ms	
<b>Ø B7</b> B7				167.695ms	
<b>d CO</b> CO		8			
	223			167.695ms	
- u u				167 605	Ĩ

Fig4-115 - Group into Bus

Select Bus Property.

😂 🖬 🎒			D1234ms - Pos:Ons	128K ▼         →14         200MH:           ▲         →1         →1         →1         →1           ▲         →1         →1         →1         →1         →1           ▲         →1         →1         →1         →1         →1         →1           ▲         Pos: 17, 102224ms         ▼         →1         →1         →1         →1	z ▼ m =	<ul> <li>50% ▼ ♣ ♣</li> <li>80% ▼ ♣ ♣</li> <li>80% ■ Height</li> <li>A - T = 17, 102224m</li> </ul>		Count 1 gger Delay 5ns B = 190,784252us +
al:167.69509m	5			085ms ~ 5 B Pos:16.91144ms  ▼		B - T = 16.91144ms		npr-Rate: 255.882
Bus/Signal	Trigger	Filter	-40	.2468ms -30.1851ms -20.1234ms -1	0.0617ms	7 Dhs 10.0617ms	20.1234ms 30.18	51ms 40.2468ms 50.30
Bus1					OXO	OX1	OX1	OX1
• A 🕫	Sampling Setu Channels Setu	-		83.884ms		13.348ms	13.442ms	13.528ms
🕑 A1 A1 📱	Bus Property			00.00485		167.695ms	10. 112003	10.02003
🥑 A2 A2	Analog Wavefo Reverse	orm	•					
A3 A3	Group into Bu		Ctrl+G			167.695ms		
	Ungroup from		Ctrl+V			167.695ms		
✓ A4 A4 —	Add Channel .					167.695ms		
🥑 A5 A5	Copy Channel					167.695ms		
🍼 <b>A6</b> A6	Delete Channe Delete All Ch					167.695ms		
✓ A7 A7	Restore Defau	ilt Channel	5			167.695ms		
🥑 BO BO	Format Row		•			167.695ms		
<b># B1</b> B1	Rename					167.695ms		
🥑 <b>B2</b> B2						167.695ms		
🥑 <b>B3</b> B3								
✓ B4 B4		<u> </u>				167.695ms		
-						167.695ms		
<b>✓ 85</b> 85						167.695ms		
🥑 <b>B6</b> B6						167.695ms		
🕑 B7 B7		$\otimes$				167.695ms		

Fig4-116 - Bus Property

Select the decoding function of the protocol analyzer HDQ and select OK to confirm.

ale:2.01234ms	() 🗰 🛛	Display			24ns 👻	Trigger Delay 5ns A - B = 190.784252us -
otal:167.69509ms Bus/Signal	Trigger	Display Filter	Aange:-50.3085ms ~ 5 B Pos:16.91144ms  ♥	B - T = 16.9114		Compr-Rate: 255.882
■ Bus1	IIIgger	Miller	Bus Property		× 0.1234ms	30.1851ms 40.2468ms 50.30 OX1
• A0 A0	x		Bus Setting	Color Config		
<b>A1</b> A1		 	Activate the Latch Function	Register	13. 442r	ns 📕 13.528ms 📕
A2 A2				Register	J	
A3 A3			Protocol Analyzer Setting			
A3 A3		~	Protocol Analyzer	Parameters Config	1	
		$\otimes$	C ZEROPLUS LA DSI Bus MODULE VI.01.00(CN01)	A and a second s	1	
🧹 A5 A5		$\otimes$	C ZEROPLUS LA FWH MODULE V1.00.00(CN02)	-		
🥑 A6 A6	$\otimes$	$\otimes$	C ZEROPLUS LA GPIB MODULE V1.00.00(CN01) C ZEROPLUS LA HD Audio MODULE V1.03.00(CN01)			
<b># A7</b> A7		$\otimes$	ZEROPLUS LA HDQ MODULE V2.07.00(CN01)			
<b># 80</b> B0		$\otimes$	<ul> <li>ZEROPLUS LA HPI MODULE V1.01.00(CN01)</li> <li>ZEROPLUS LA I2C(EEPROM 24LC561/24LC562) MODUI</li> </ul>	E V1.00.00(CN01)		
<b>61</b> B1 B1			<ul> <li>ZEROPLUS LA I2C(EEPROM 24L) MODULE V1.31.00(CP</li> <li>ZEROPLUS LA I2C MODULE V2.02.00(CN01)</li> </ul>			
<b>6 B2</b> B2				<u>•</u>	!	
		$\otimes$	✓ Use the DsDp	Find		
🧹 B3 B3		$\otimes$	More Protocol Analyzer			
🥑 B4 B4	$\boxtimes$	$\otimes$	ОК	Cancel Help		
🥑 85 85		$\otimes$		167. 6951	ns	
🥑 B6 B6		$\otimes$		167. 695r	ns	
<b># 87</b> 87		$\otimes$		167. 695r		
<b>d</b> CO CO	87			167.605-		

Fig4-117 - Protocol Analyzer HDQ Setup

Complete the protocol analyzer HDQ decoding.

Busi (HDQ)         Image: Constraint of the second sec	ccer     Filter       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S       X     S	19. 12200mm         19. 40014mm         19. 696934mm         14. 27514mm         14. 361355mm         14. 851565mm         15. 19776mm         15. 427966mm         15. 7161           Unikution         Break         Address         CX62         Read         Data         CX18           13. 348ms         207. 6         167. 695ms         167. 695ms         167. 695ms         167. 695ms           167. 695ms         167. 6
A0 A0     A0     A1 A1     A2 A2     A3 A3     A4 A4     A5 A5     A6 A6     A7 A7		Unknow         Break         Address         : 0X62         Read         Data         : 0X18           13. 348ms         207.6         167. 695ms         167. 695ms <t< th=""></t<>
A1     A1       A2     A2       A3     A3       A4     A4       A5     A5       A6     A6       A7     A7		167. 695ms 167. 695ms 167. 695ms 167. 695ms 167. 695ms 167. 695ms 167. 695ms
A2         A2           A3         A3           A4         A4           A5         A5           A6         A6           A7         A7		167. 695ms 167. 695ms 167. 695ms 167. 695ms 167. 695ms
A3         A3         A3           A4         A4         A4           A5         A5         A5           A6         A6         A6           A7         A7         A7		167.695ms 167.695ms 167.695ms
A4 A4     A4     A5 A5     A6 A6     A7 A7		167. 695ms 167. 695ms
<ul> <li>A5 A5</li> <li>A6 A6</li> <li>A7 A7</li> </ul>		167.695ms
A6 A6     A7 A7	X 🛛	
✓ A7 A7		167 605mg
		101.000m3
<b>✓ BO</b> BO		167.695ms
	8 8	167.695ms
	X 🛛 🛛	167.695ms
🥑 B2 B2		167.695ms
🥑 B3 B3	x 🛛 🖉	167.695ms
of B4 B4	x 🛛	167.695ms
		167.695ms
		167.695ms
<b>Ø B7</b> B7	8 🛛	167.695ms

Fig4-118- Protocol Analyzer HDQ Decoding



PROTOCOL ANALYZER HD	λQ			×
Configuration Packet [	Data Format   Register			
Item	Color	ltem	Color	
🔽 Break		🔽 Write		
Recovery		🔽 Describe		
Address				
🔽 Data				
🔽 Read				
		OK	Cancel Default	Help

# 4.5.6.2 Protocol Analyzer HDQ Packet Analysis

Fig4-119 - Protocol Analyzer HDQ Packet dialog box

**Item:** Select the content which needs to display in the Packet List, which includes Break, Recovery, Address, Data, Read, Write and Describe.

Color: Set color for items which needs to display in the packet list.



# 4.5.7 CAN 2.0B Analysis

### Preface

Add Protocol Analyzer function to analyze CAN 2.0B transport protocols data. CAN 2.0B serial transmission, there are two signal channels, CANH and CANL, which match with baud ratio judge serial data. If you want to change serial data into Bus format, you need to analyze this function with LA. a dialog box needs to be added; you should set up a Protocol Analyzer CAN 2.0B dialog box.

# **CAN 2.0B Introduction**

### **1. Brief Introduction**

### Features

CAN 2.0B (Controller Area Network) is an Asynchronous Transmission Protocol. It costs low, sky-high use rate, far data transmission distance (10KM), very high data transmission bit (1M bit/s), sending information without appointed devices according to message frame, dependable error disposal and detection error rule, message automatism renewal after damage, and node can exit Bus function on the serious error .

### Applications

CAN 2.0B is used for automotive electronics correlation systems connection.

### 2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	CAN 2.0B
Required No. of Channels	1
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz
Appropriate Sampling Rate	100MHz
Same Data Time Per Bit	⊡Yes ∎No
Name of Syn. Signals	CAN 2.0B
Data Verification Point	Low signals $>$ 190us converts to High signals $>$
	40us

### 3. Protocol Analyzer IO Description

Function
The main signal source of transmission data
Signal is opposite to the signal source of transmission data

### 4. Protocol Analyzer Electrical Specifications

Parameter	Min.	Туре	Max.	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

# **CAN 2.0B Frame Specification**

CAN 2.0B can separate into frames as follows: Data Frame, Remote Transmit Request Frame, Error Frame, Overload Frame. Because CAN2.0B is transmitted by the format of different signals, the signal can separate into CANL and CANH, and the signal direction of CANH is opposite to that of CANL. Next we analyze CAN 2.0B signal with the standard of CANL.

## **Basic Data Frame**

Data frame can be divided into Basic CAN and Peli CAN, Data Frame of Basic CAN transmission. As follows,



message data can be separated into Start of Frame (SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame.

Arbitration Field	Control Field	Data Field	CRC Field	Ack End of Field Frame
	8			

Fig4-120 - Basic Data Frame

## Start of Frame

Every Start of Frame must be 0, which means asking far data to come back.

### **Arbitration Field**

Identifier is 11bits; its function is the sequence when transmitting signal, numerical value is lower, the priority is higher, and the array is from ID-10 to ID-0, and the numerical value is not all from ID-10 to ID-4, finally RTR(Remote Transmit Request) is the judgment bit of transmission or Remote Transmit Request. When RTR=0, it denotes that the data goes out; when RTR=1, it means asking far data to come back.

# **Control Field**

Control Field consists of 6 bytes, including Data Length Code and two Reserved Bits as Peli frame for future expansion. The transmission reserved bit must be 0. Receiver receives all bits combining 1 with 0. As the below figure, IDE and RB0 of Control Field are Reserved Bits which must be 0 and the latter 4bits are only 0-8 which denotes the data behind will transmit several bytes data.

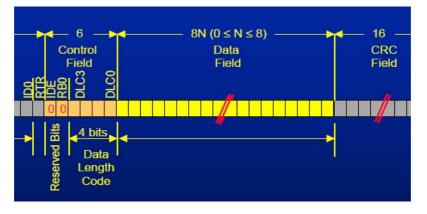


Fig4-121 - Control Field

## **Data Field**

The Data Field consists of the data to be transferred within a Data Frame. It can contain from 0 to 8 bytes, and each contains 8 bits which are transferred MSB first.

## **CRC** Field

16bits CRC, the last is a delimiter, and the default is 1.

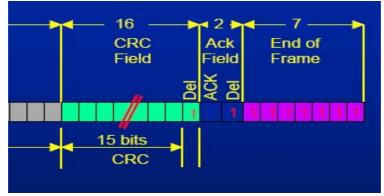


Fig4-122 - CRC Field

# Ack Field

That is the return signal of Receiver, which has 2 bits, and the final is a delimiter whose default is 1. If receiving success, Ack will send back 0, then the transmitter knows the Receiver has received the data.

## **End of Frame**

1111111 denotes en

## Peli Data Frame

In the Peli Data frame, Data Frame as follows, the frame of message is separated into Start of Frame (SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame. However, the parts of Arbitration Field have much more than 18bits and the SRR and IDE are 1.

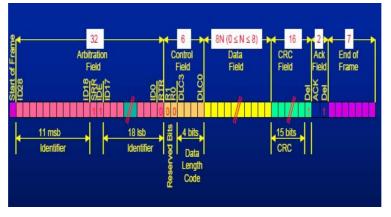


Fig4-123 - Peli Data Frame

# **Remote Transmit Request Frame**

When RTR=1, it denotes Remote Transmit Request Frame, at this time, DLC3...DLC0 are the Data bytes of return data. And the frame doesn't have Data Field.

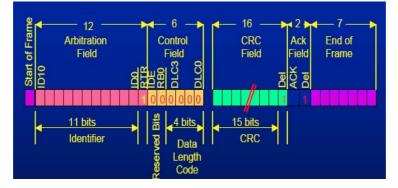


Fig4-124 - Remote Transmit Request Frame



### **Error Frame**

The Active Error Flag consists of six consecutive Data Field 'dominant'bits. Dominant bits violate the law of bit stuffing. All bits can produce Error Frame after recognizing bit stuffing wrong, the Error Frame called Error. Corresponding Error Flag Field includes sequence bits from 6 to 12 (which produces by 1 or more nodes). Error Frame ends in Error Delimiter field. After Error Flag sends out Bus actively to get the right state, and the interrupted node tries its best to send abeyant message Error Delimiter. Error Delimiter consists of eight 'recessive' bits and allows Bus node to restart Bus transmission after Error happens.

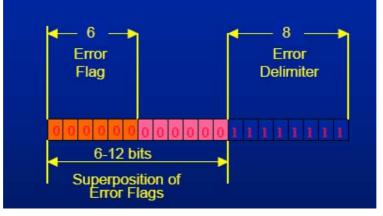


Fig4-125 - Error Frame

# **Overload Frame**

There are two kinds of Overload conditions, which both lead to the transmission of an Overload Flag. The internal conditions of a node which require a delay of the next Data Frame start during the first bit of Intermission. Overload Flag can send six '0', which may damage Intermission format so that it makes the other nodes know node sending Overload Flag at this time. When Overload Flag is sent out, Overload Delimiter can send eight '1', others send seven '1'after finishing either.

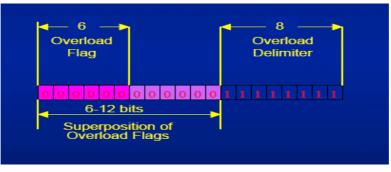


Fig4-126 - Overload Frame

### **Interframe Space**

Interframe Space is divided into Intermission and Bus Idle. Intermission is three '1'. It is impossible to send any message during this time, except Overload Frame. The Bus is recognized to be free; the period of BUS IDLE may be of arbitrary length. And any station having something to transmit can access the Bus. When a node is at the state of 'error passive', the node will send eight '0' after INTERMISSION and other node have the chance to retransmit themselves information.



### 4.5.7.1 Software Basic Setup of Protocol Analyzer CAN 2.0B

PROTOCOL ANALYZER CAN 2.0B	×
Configuration Packet Data Format Register	
Pin Assignment Start Packet Format	
Protocol Analyzer Name: Bus1       111Bit Start	
Channel: A0 O Bit Start	
Protocol Analyzer Property	
Percentage Sample:       60%         Baud Rate:       125000         (Min:1bps,Max:10Mbps)       Auto         When CAN Data for expansion,combine Basic ID and ID         The Del is displayd in the CRC Field	
Protocol Analyzer Color Start Control CRC Error ACK	
End ID Data Overload NACK	
OK Cancel Default Help	

Fig4-127 - Protocol Analyzer CAN 2.0B Configuration dialog box

#### Set the CAN 2.0B Configuration dialog box

#### **Pin Assignment:**

Protocol Analyzer CAN 2.0B only needs one channel to decoding signals, the default channel is A0.

**Start Packet Format:** The Start Position can be divided into two formats, 111 Bit Start (the Start Position is that three bits are High.) and 0 Bit Start (the Start Position is that one bit is Low).

#### **Protocol Analyzer Property:**

**Percentage Sample:** The Percentage Sample should be entered in the position of the Baud Rate which is selected from the range between 25% and 75%, and the default of the Baud Rate is 60%. The resolution can be adjusted to 1%.

**Baud Rate:** The Baud Rate can be set to Integer or selected from the pull-down menu (10000, 20000, 400000, 500000, 800000, 1250000, 2000000, 2500000, 4000000, 5000000, 6600000, 8000000 and 10000000) manually, and the default is 125000. If the Auto is selected, the Baud Rate can be calculated by the main program automatically and displayed on the CAN 2.0B dialog box.

Data Reverse Decoding: If it is selected, the data can be decoded in reverse.

After End Packet happens, just begin to analyze: If it is selected, the signal will be decoded when the End Packet appears.

When CAN Data for expansion, combine Basic ID and ID: If the option is selected, the Basic ID and ID will be combined.



The Del is displayed in CRC Field: If it is selected, the Del will be displayed in the CRC Field.

#### **Protocol Analyzer Color:**

The protocol analyzer colors can be varied by users.

### **Operating Instructions**

Turn on the user interface of the Logic Analyzer.

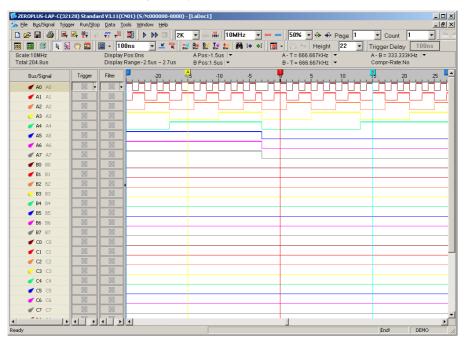


Fig4-128 - User Interface

STEROPLUS-LAP-C (32128) Standard V3.11 (CH01) (S/H:000000-0000) - [CAH2.0B] - 🗆 🗵 or file by:/Signal Trigger Run/Stop Data Iools Yindow Help D 😂 📓 🚔 💐 40 v 🚓 🖓 🗓 D ト ト □ 128K v 🗱 1000 HHz v mov - 8 × 10% 💌 🚸 孙 Page 1 ▼ Count 1 • 
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 □
 A - B = 16.182424us -Compr-Rate:255.883 1 Uns Bus/Signal Trigger 48. 682703us 97. 365407us 146. 04811us 194. 730814us243. 413517us292. 096221us340. 778924 🕑 A0 A ×  $\otimes$ 🕑 A1 🛛 A1  $\boxtimes$  $\otimes$ 🥑 A2 A2  $\otimes$  $\otimes$ 🥑 A3 A3  $\otimes$  $\boxtimes$ 🥑 A4 A4  $\boxtimes$  $\otimes$ ✓ A5 A5  $\otimes$  $\otimes$ 🥑 A6 🛛 A6  $\boxtimes$  $\otimes$ ✓ A7 A7  $\otimes$  $\otimes$ **€ 80** 80  $\otimes$  $\otimes$ ПГ П **# 81** B1 🥑 **B2** B2  $\otimes$  $\otimes$ 🥑 B3 B3  $\boxtimes$  $\otimes$ 🥑 **B4** B4  $\otimes$  $\otimes$ 🥑 85 BS 🥑 B6 B6  $\otimes$  $\otimes$ **♂ 87** 87  $\mathbb{X}$  $\otimes$ 🥑 CO 🛛 🕬  $\boxtimes$  $\otimes$ • Þ End! DEMO

Sample the CAN 2.0B signal or open the sampled waveform.

Fig4-129 - CAN 2.0B Waveform

Group the signal channels into Bus.

				(S/N:000000	-0000) - [C <i>l</i>	M2.0B]					_ 🗆 ×
5 File Bus/S											_ B ×
🗋 🗅 📂 📓 🖉		🖞 🕂 🖓 🖓	1	bb 🗆 🛛 120	BK 💌 🏭 🔤	200MHz	• no and 10	)% 🝷 👬 🔺	Page 1	▼ Count 1	- <u>-</u> fa f
🖼 📰 🥵	🔺 🔛 🖑	🛗  🗃 📲 🤋	.736541u	- 👗 🦞 🚦	AN BAR BAR BAR	👬 👸 😽	🌒 🛛 📓 📲 🔡	e Height	30 -	Trigger Delay	5ns
Scale: 9.7365			y Pos:194.7		A Pos:87.8			= 87.851299u		A - B = 16.182424	
Total: 167.695	579ns	Displa	y Range:-48	3.682703us ~			B - 1	= 104.033724	15 🔻	Compr-Rate:255.88	3
Bus/Sign	al Tri	gger   Filter		0ns 48.	682703us 97.36	B 53407us 146.04	811us 194. 730814	us243. 413517us	292. 096221u	340. 778924us389. 46162	8u:438. 14433
🖌 A0 🚽	L Sampling Se	· · · · · · · · · · · · · · · · · · ·	╴╢═╧╧╧╧						<u></u>		
	🕻 Sampiing Se 🐍 Channels Se				<u> </u>	<u>-</u>		U			
	US Bus Propert										
🥑 A2 🥈	Analog Wave		•								
🧹 A3	Reverse										
🥑 A4	Group into		Ctrl+G								
•	Ungroup fro	m Bus	Ctrl+U								
🍼 A5	Add Channel										
🍼 A6	Copy Channe										
# A7	Delete Chan Delete All		-								
<b>a</b> 80		ault Channels		h							I
<b>•</b> BU	Format Row										
✓ B1	Rename										
🍼 B2 B	2	8 🛛 🛇									
🥑 ВЗ В	з р										
<b>♂ B4</b> B	4 5		1								
<b>Ø 85</b> B											
<b>✓</b> B6 B											
-	×		_	_							
<b>€ 87</b> B	7										
€00	:0 [2	8 🛛									
											<b>_</b>
Ready										End!	DEMO
neardy										Janai	DEMO ///

Fig4-130 - Group into Bus

Select the **Bus Property** to set up the Bus Property dialog box .

	(32128) Standard V3.11(CH01) . Trigger Run/Stop Data Tools	(S/H:000000-0000) - [CAM2.0B]
) 😂  😂 🛛	R R 😳 🐢 🐺 🕫 🔟 🕨	▶ 🔲 128K V 🚧 🔲 200MHz V 🗤 10% V 🌾 🐳 Page 1 V Count 1 V
3 🖽 🥵 🖹	📓 🖑 🛅 📓 - 9.736541u:	▼ 🤐 💦 🔐 🔐 🔡 🎜 👪 10 of 🔞 - 📴 00 Height 30 💌 Trigger Delay 5ns
cale:9.736541us otal:167.69579ms	Display Pos: 194.73	
otal:Ibr.095r9ms	Display Kange:"40.	
Bus/Signal	Trigger Filter	ons 48.682703us 17.865407us 146.04811us 194.730814us243.413517us292.096221us340.778924us389.461628us438.1443
Busi	ii Sampling Setup	V 0X1 )(/ 0X1 )(/ 0X1 )(/ 0X1 )(/ 0X1 )(/ 0X1 )(/ 0X1 )(/ 0X0 )( )()()()(/ (X))
	💑 Samping Setup	
🖌 A1 A1	Bus Property	
✓ A2 A2	Analog Waveform Reverse	
A3 A3	Group into Bus Ctrl+	+0
-	Ungroup from Bus Ctrl+	
🥑 A4 A4 -	Add Channel	
🧹 A5 A5	Copy Channel	
🥑 A6 A6	Delete Channel Delete All Channels	
✓ A7 A7	Restore Default Channels	
<b>60</b> B0	Format Row	
-	Rename	
ɗ B1 B1 ─		
🥑 <b>B2</b> B2		
🥑 <b>B3</b> B3	$\otimes$	
🥑 B4 B4		
<b>65</b> 85		
✓ B6 B6		
✓ B7 B7		
-		
<b> co</b> co	N 4 7 N 4 7 N 4	

Fig4-131 - Bus Property

Select the decoding function of the protocol analyzer CAN 2.0B and select OK to confirm.

🚺 ZEROPLUS-LAP-C (32 🍒 File Bus/Signal 1			1(CH01) (S/H.00000-0000) - [CAH2.0B]
		e <b>or o</b> n lar	
			36541u: ▼ 😹 💘 📰 🎎 👪 🐇 🗰 10 01 🔞 ▼ 💾 20 Height 30 ▼ Trigger Delay 5ns
Scale: 9, 736541us			Substitut v mm K mm for far far far far far far far far far fa
Total:167.69579ms			Range:-48.682703us ~ B Pos:104.033724us 💌 B - T = 104.033724us 💌 Compr-Rate:255.883
Bus/Signal	Trigger	Filter	
▼ Bus1	-	× 🛛	
• A0 A0	x	$\otimes$	Color Config
🝼 A1 A1		$\otimes$	Activate the Latch Function     Register
✓ A2 A2		$\otimes$	
🧹 A3 A3	$\boxtimes$	$\otimes$	Protocol Analyzer Setting
🥑 A4 A4	$\boxtimes$	$\otimes$	Protocol Analyzer     Parameters Config
<b>as</b> as	$\boxtimes$	$\otimes$	C ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01)
🥑 A6 A6	×	$\otimes$	C ZEROPLUS LA AG97 MODULE VI.02.00(CN01) C ZEROPLUS LA ARITHMETICAL LOGIC MODULE VI.51.00(CN01)
<b>₫ A7</b> A7	×	$\otimes$	C ZEROPLUS LA BDM MODULE V1.00.00(CN01) C ZEROPLUS LA BUS MODULE V1.00.00(CN01)
<b># 80</b> 80		$\otimes$	CZEROPLUS LA CON 2.08 MODULE VI 32.00(CN01)     CZEROPLUS LA CON 2.08 MODULE VI 32.00(CN01)
<b># 81</b> B1		$\otimes$	C 2EROPLUS LA COMPACT Flash A1 MODULE V1.01.00(CM01)
<b>6 B2</b> B2		$\otimes$	✓ Use the DsDp     Find
🥑 <b>B3</b> B3	×	$\otimes$	More Protocol Analyzer
<b>♂ 84</b> 84	×	$\otimes$	OK Cancel Help
✓ 85 85		$\otimes$	
<b># B6</b> B6		$\otimes$	
<b>Ø 87</b> 87		$\otimes$	
<b>~ co</b> co			
Ready	اغر المربي :	الغالصي	Endi DEMO

Fig4-132 - CAN 2.0B Bus Property Setup

Double click the ZEROPLUS LA CAN 2.0B MODULE V1.32.00 (CN01) to set the Protocol Analyzer CAN 2.0B dialog box.

PROTOCOL ANALYZER CAN 2.0B	x
Configuration Packet Data Format Register	
Pin Assignment	Start Packet Format
Protocol Analyzer Name: Bus1	111Bit Start
Channel:	O 0 Bit Start
Protocol Analyzer Property	
Percentage Sample: 60%	Data Reverse Decoding After End Packet happens, just begin to analyze When CAN Data for expansion,combine Basic ID and ID The Del is displayd in the CRC Field
Protocol Analyzer Color Start Control CRC	Error ACK
End ID Data	Overload NACK
ОК	Cancel Default Help

Fig4-133 - Protocol Analyzer CAN 2.0B Setup



Click OK in the Protocol Analyzer CAN 2.0B dialog box to complete the CAN 2.0B Setting.

🐝 ZEBOPLUS-LAP-C (32	128) Stan	dard V3.1	1(CH01) (S	/ <b>#</b> :0000	00-0000) -	- [CAN2.	08]					
🂪 <u>F</u> ile B <u>u</u> s/Signal T												_ 8 ×
🗅 😂 🖶 🎒 🔍	🕰 💱   🐗	₽ <b>₽₽</b> •[1]		▶ □   [·	128K 💌 👬	• 🐳 🛛 🛛	JOMHz 💌	<u></u> 10	% 🔻 🧄 🗕	Page 1	▼ Count	1 💽 🚠 🖬
💌 📰 🤔 🖹 🕅	 (*) 🛅	🐺 🖌   9.7	36541 u: 🔻	K K		2 <b>T⊻ +2</b> F Bar Bar	🙀 14 🔿	🐻 - 📴	🔖 Heigh	nt 30 💌	Trigger Delay	5ns
Scale: 9. 736541us			Pos:194.7308 Range:-48.68			:87.85129			= 87.851299		A - B = 16.182	
Total:167.69579ms		Display	Kange: -48. 68	52703us	B Pos	104.0337	24us   🔻	B - T	= 104.03372	4us 🔻	Compr-Rate:255	. 883
Bus/Signal	Trigger	Filter	<b>.</b>	)ns	48.682703us	97. 36540	7us 146.04811	us 194. 730814	us243. 413517	us292. 095221us	340. 778924us389. 46	1628us438.14433
Bus1 (CAN 2.08	-	⊗ •	Unknow	Basi	.c ID : )	OX7FF		ID : 0X	3FFFF		0X2 0X	.53 (0X32
• A0 A0	x	$\otimes$		[]								
🝼 A1 A1		$\otimes$										
✓ A2 A2	X	$\otimes$										
🧹 A3 A3		$\otimes$										
✓ A4 A4	X	$\otimes$										
✓ A5 A5		$\otimes$										
🥑 A6 A6	$\square$	$\otimes$										
✓ A7 A7		$\otimes$										
🥑 BO BO		$\otimes$										
<b>♂ B1</b> B1		$\otimes$										
🥑 <b>B2</b> B2		$\otimes$										
🥑 <b>B3</b> B3		$\otimes$										
		$\otimes$										
🥑 B5 B5		$\otimes$										
🥑 <b>B6</b> B6		$\otimes$										
<b># B7</b> B7		$\otimes$										
✓ C0 C0			4									▼ ▶
Ready			_								End!	DEMO //.

Fig4-134 - CAN 2.0B Decoding



PROTOCOL ANALYZER CA	N 2.0B			×
Configuration Packet [	)ata Format   Register	1		
Item	Color			
Control				
🗹 Data				
IZ ACK				
NACK				
🔽 Describe				
	OK	Cancel	Default	Help

# 4.5.7.2 Protocol Analyzer CAN 2.0B Packet Analysis

Fig4-135 - Protocol Analyzer CAN 2.0B Packet dialog box

Packet color can be varied by users.

The Packet displays with the waveform as below:

SEROPLUS-LAP-C (321				2.08]			
🏂 Eile Bus/Signal Tri			128K ▼ ₩4 ₩	200MHz 🔻 🗤			
		1 🔟 🕨 🕨 💷 1 1.736541 u: 🕶 🌿 😤				Page 1 Co 30 V Trigger	unt 1 💽 👍 🖬
Scale: 9. 736541us		v Pos: 194. 730814us	A Pos:87.851		A - T = 87.851299us		Delay 5ns 16.182424us -
Total:167.69579ms	Displa	y Range:-48.682703us ~			B - T = 104.033724us	▼ Compr-Ra	te:255.883
Bus/Signal	Trigger Filter	Dins .	48.682703us 97.365	407us 146. 04811us 1	94. 730814us243. 413517us2	92. 096221us340. 778924u	s389. 461628uz438. 14433
Bus1 (CAN 2.06	• 🛛	• (Inknow ) Basi	c ID : OX7F		ID : OX3FFFF	OX2	0X53 0X32
• A0 A0	X 🛛						
🝼 A1 A1							
🧹 A3 A3							
✓ A4 A4							
✓ A5 A5							
✓ A6 A6							
✓ A7 A7							
<b>60</b> B0							
<b>d B1</b> B1							-
							Þ
× Setting Refresh	Export Synch P	Parameter	31	EX RE OV ER			
			GRR IDE ID	RTR RB1 RE		ACK DESCRIBE	<u> </u>
1 Bus1(CA/	N 2.0B) Or	ns 7FF 9	GRR IDE 3FFFF	RTR RB1 RE	30 2 53 32 E9AB	ACK Extend	
Ready						End!	DEMO
Accuy						jana:	DEMO //

Fig4-136 - CAN 2.0B Packet List Displayed with the Waveform



# 4.6 Compression

The compression function enables the system to compress the received signal and has more data stored in per channel.

## 4.6.1 Software Basic Setup of Compression

Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.

- Step2. Set up the trigger edge on the signal or the Bus to be triggered.
- Step3. Click 🔟 icon, or click the compression function from the Sampling Setup dialog box then click Apply and OK to run.

	Sampling Setup	×
	Clock Source Asynchronous Clock	
Image: Signal       Trigger       Run/Stop       Data         Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup         Image: Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup         Image: Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup         Image: Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup       Image: Sampling Setup	Synchronous Clock    External Clock	
Image: Signal Filter Setup         Scale:         Total:2         Group into Bus         Ungroup from Bus         Ctrl+U         E         Expand         Collapse	Sampling RAM Size RAM Size: 2K  Compression Mode Data Compression Channel number will be limited to 32	
Format Row   Rename	Apply OK Cancel Restore Defaults Help	

Fig 4-137 – Compression Mode

**Step4.** Click **Run**, and then activate the signal from the tested circuit to acquire the result on the waveform display area. Fig 4-138 shows the result before and after compression has been applied.

EROPLUS-LAP-C (3 File Bus/Signal				00001) - [LaDoc1						_
				, 🔽 🗟 👪 100		<b>50%</b>	h ali Pere	1	- Count 1	
				- Ar Br Br Dar Dar						
ale:10ns		•    TOHS Display Pos:Ons		A Pos:-150ns 🖛		A - T = 150ns			- B = 300ns	
otal:20.48us	I	Display Range:-	250ns ~ 270ns	B Pos:150ns 💌		B - T = 150ns	<b> </b> •	Co	mpr-Rate:No	
Bus/Signal	Trigger F	'ilter 📕	-200ns -	A T50ns -100ns	-50ns 0	ins 50n:	100ns	B 150	ns 200n	s 250n
🥑 AO AO					Unknown					
<b>41</b> A1					Unknown					
A2 A2					Unknown					
A3 A3					Unknown	<u> </u>				
						ļ				
🥑 A4 A4					Unknown					
🥑 A5 A5	$\boxtimes$				Unknown	-				
🥑 A6 A6					Unknown	-				
✓ A7 A7		⊠.			Unknown					
<b># 80</b> B0					Unknown					
<b>61</b> B1 B1					Unknown					
✓ B2 B2					Unknown					
-					Unknown					
🥑 B3 B3						1				
🥑 B4 B4					Unknown					
🥑 85 85					Unknown	-				
🍼 B6 B6					Unknown					
<b># 87</b> 87					Unknown					
<b>d CO</b> CO					Unknown					
					Unknown					
- CI CI	<b>F 4   F 4</b>	िमन		+	ormitowit	1				

		11(CM01) (S/W:00000000 ta Tols Mindow Help	01) - [LaDoc1]				
Elle Dus/Signal			▼ 🛤 👪 100MHz	× m m 50% × d	and Page 1	▼ Count 1	-
							10ns
ale:10ns (tal:205.23us	Display	Pos:Ons	A Pos:-150ns V B Pos:150ns V	A - T = 150ns B - T = 150ns	-	A - B - 300ns V Compr-Rate:10.021	
Bus/Signal	Trigger Filter	-200ns -150	ns -100ns -50n	s Ons 50ns	100ns	B 150ns 200ns	250ns
🝼 AO AO	× • × •			snown			
🝼 A1 A1			Unl	known			
🥑 A2 A2			Unl	known			
🥑 A3 A3			Unl	known			
🥑 A4 A4			Unl	known			
🥑 A5 A5			Unl	known			
🥑 A6 A6			Unl	known			
✓ A7 A7			Unl	known			
<b># BO</b> BO			Unl	known			
<b>d B1</b> B1			Unl	known			
<b>€ B2</b> B2			Unl	known			
🥑 <b>B3</b> B3			Uni	known			
🍼 B4 B4			Uni	known			
🥑 B5 85			Unl	known			
🥑 B6 B6			Unl	known			
<b>ø 87</b> 87			Unl	known			
✓ C0 C0			Unl	known			
<b>∕ C1</b> C1			Unl	known			
	• • • • • •					End! Con	nected

Fig 4-138 – Before and After Compression

Using 2K memory depth, before Compression has been applied, the total of the data was 20.48us; after the Compression had been applied, the total of the data was 205.23us, therefore, the compression rate is 10.021.

Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

Step5. Click the compression icon again or click off the compression function to stop compression.

Tip: Compression cannot be applied with the signal filter function at the same time.



# 4.7 Signal Filter and Filter Delay

The function of the Signal Filter and Filter Delay allow the system to keep the required waveform, and filter out the waveforms that aren't required.

### 4.7.1 Basic Setup of Signal Filter and Filter Delay

Software Basic Setup of Signal Filter and Filter Delay

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Set up the trigger edge on the signal or the Bus to be triggered.
- **Step3.** Click Replace icon, or click the Signal Filter Setup button on the Sampling Setup dialog box or select the item form the pull-down menu of the Bus/Signal and then the Signal Filter Setup dialog box will appear.

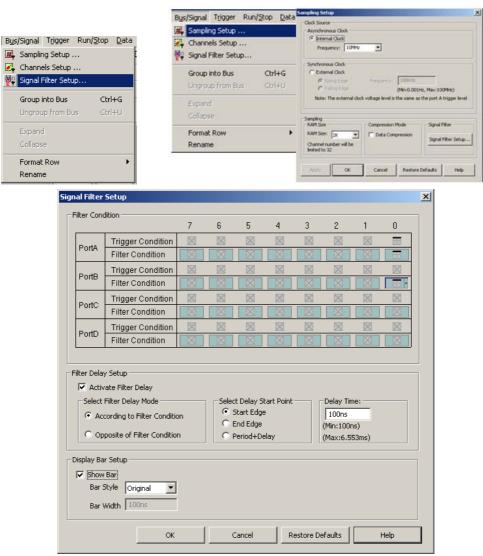


Fig 4-139 – Signal Filter Setup

Set the high level as Filter Condition on the signal A1.

#### Step4. Signal Filter Setup

- 1. Setup the Filter Condition as 📰 or 🖳 on the signal to be analyzed.
- 2. Click OK, then click Run to activate the signal from the tested circuit to the Logic Analyzer.

3. The system will display only the waveforms of the signals which are qualified by the Filter Condition.

Bus/Signal	Trigger	Filter		
or ao 🗸 🖌	Z	$\boxtimes$	311. 795us <u>15. 8</u>	8 30. 525us 20. 4us
🝼 A1 A1		•	309. 055us	
🍼 A2 A2		$\boxtimes$		655.36us
🥑 A3 A3				655.36us
of A4 A4				655.36us
🥑 A5 A5				655.36us
🥑 A6 A6		$\boxtimes$		655.36us

Bus/Signal	Trigger	Filter	
🖌 AO AO			<u>#118.27us</u>
🝼 A1 A1			<u>x</u> 388.33us
🍼 A2 A2			<u>x</u> 388.33us
🥑 A3 A3			7 388. 33us
🥑 A4 🗛			<u>v</u> 388. 33us
🥑 A5 A5			7 388.33us
🥑 A6 A6			7 388. 33us

Fig 4-140 – Without/With Signal Filter Setup

The first picture shows the result without any signal filter setup.

The second picture shows the result which has set the high level on the Filter Condition of the signal A1. Only the waveform with the high status of A1 is displayed.

Step5. Filter Delay Setup

- 1. Click on the Activate Filter Delay as shown in Fig 4-141.
- Click on the According to Filter Condition or the Opposite of Filter Condition to select the waveforms to be kept.
- 3. Click on the Start Edge, End Edge or Period + Delay to set the Start Point of Filter Delay.
- 4. Type the value of the Delay Time into the column of the Delay Time.
- 5. Click OK, then click Run to activate the signal from the tested circuit to the Logic Analyzer.
- 6. The result will be displayed in the waveform display area as shown in Fig 4-140.
- Step6. Stop Signal Filter/ Filter Delay

Click **Stop**, then click **Signal Filter Setup** and select **Cancel** from the Signal Filter Setup dialog box to stop the Signal Filter or the Filter Delay Setup.

- Tip: Click Stop to check the conditions of the Signal Filter or the Filter Delay Setup, if there aren't any results.
- Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

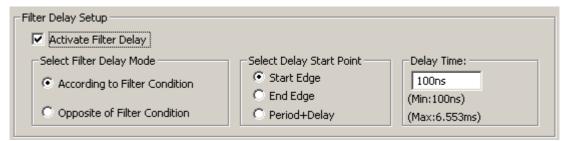
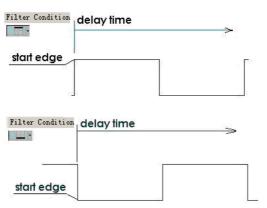
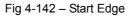


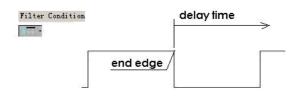
Fig 4-141 – Filter Delay Setup



**Tip:** Definitions of the **Start Edge** and the **End Edge** and the **Period + Delay** are listed as Figs 4-142, 4-143, 4-144 and 4-145.

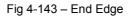


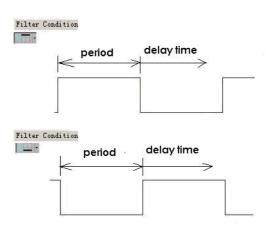


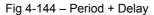


Filter Condition









② 孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.
---

6 38		7	6	5	4	3	2	1	0
PortA	Trigger Condition								7
	Filter Condition			NTR.	RC28	23	231	8728	10101 82725
PortB	Trigger Condition Filter Condition								
9									
PortC	Trigger Condition Filter Condition								
	Trigger Condition			X		X	N.		X
PortD	Filter Condition								×x
ilter Dela									
Select	y Setup ate Filter Delay Filter Delay Mode cording to Filter Conditi posite of Filter Conditic		0 s 0 s	t Delay Si Start Edge End Edge Period+De	•		Delay Tin 1s (Min:100r (Max:6.55	s)	

Fig 4-145– Filter Delay Setup

The delay time of signal A0 is 1 us, which is the condition of the Filter Delay Setup.

Step 7. Signal Filter Time Interval

1. Click Show Bar to know the length of the tested and deleted signal as shown in Fig4-146 below.

Display Bar Setu	q.						
🔽 Show Bar							
Bar Style	Original	•					
Bar Width	100ns						
		ОК	Cancel	Restore	e Defaults	Help	
							•

Fig4-146 - Display Bar Setup

2. The bar has two styles, which are Original and Bar; the default is Original style, which denotes the bar function cannot be used. When selecting Bar style, the bar function can be activated.

- 3. Bar Width, when Bar style is selected, the bar width can be set by users.
- **Tip:** The minimum bar width is 1; the maximum bar width is 65535. If the value exceeds the range, or the font is not according to the requirement, a tip window will appear.

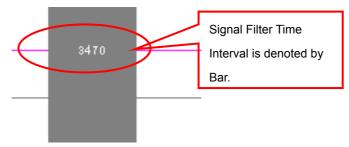


Fig4-147 - Signal Filter Time Interval



Tip: The Signal Filter Time Interval is limited under the following situations:

A: The Filter Delay and Display Bar of Signal Filter are not available under the compression mode.

B: The Filter Delay and Display Bar of Signal Filter are not available under the double mode.

C: The final two data are NULL.

D: Logic Analyzer supports the Signal Filter Time Interval function on condition that the time interval between signal filter must be more than two clocks.



# 4.8 Noise Filter

The Noise Filter function enables the system to filter the waveform that doesn't meet users' requirements.

## 4.8.1 Basic Software Setup of Noise Filter

STEP1. Click **Data** on the Menu Bar, then select 2 Noise Filter to activate the noise filter function as the figure below.

<u>D</u> ata	<u>T</u> ools <u>W</u> indow <u>H</u> elp			
<b>  </b>   =	Select an Analytic Range		Noise Filter	×
atar 🗈	Voise Filter			
23 8	Bus Width Filter		Noise Filter: None	
T .	Data Contrast		Noise Filter: None	
F	Find Data Value	Ctrl+F	OK Cancel	
F	Find Pulse Width			

Fig4-148 - Noise Filter

### STEP 2.Transmit the tested signal to the Logic Analyzer as the figure below.

Bus/Signal	Trigger	Filter	۲	н Т.	1	1	20 20	1 1		÷	. <del>.</del> .		E.	4	10		i i			5	80.6			ł		. 1	от 10
🖌 AO AO	•		1	1 1	1	1	1 1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	2	1	1	1	1	1	1 1
🝼 A1 A1			2	2	1	2	2	2		2		2	Ī	2	1	2	2		2	5	1	2	ſ	24	2		2
<b>∉ A2</b> A2				4		4	4		4	ŧ		1	4			4	ŀ			3			4		[	4	
🥑 A3 A3					8			1			8	1						7							8		

Fig4-149 - Tested Signal

STEP 3.Filter waveforms that are not bigger than 5 clocks.

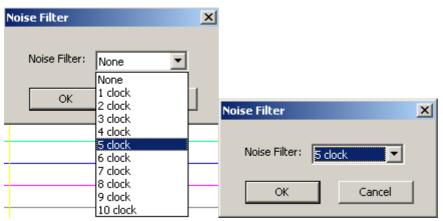


Fig4-150 - The condition of Noise Filter is 5clock.

STEP 4. After filtering, the waveforms that are not bigger than 5 clocks are deleted.

Bus/Signal	Trigger	Filter	<mark>-</mark>	 <mark>위</mark> 	-10 -5	 	5 10 	15 20
🝼 AO AO	•					20		
🝼 A1 A1						20	48	
<b>∉ A2</b> A2						20	48	
🥑 A3 A3			8	8	7	8	8	8

Fig4-151 - Waveforms after Filtering

STEP 5. Reserve the original waveform: open the Noise Filter window, and then select None, the waveform will be restored.

Noise Filter		×
Noise Filter:	None	[
	None	
ОК	1 clock 2 clock	
	3 clock	- 1
	4 clock	
	5 clock	
	6 clock	
	7 clock	
	-8 clock	
	9 clock	
	10 clock	

Fig4-152 - Restore the Waveform



## 4.9 Data Contrast

In order to make users analyze the Data and contrast the difference of Data easily, there are adding the function of Data Contrast. The function of Data Contrast is used to compare the difference of two signal files of the same type. One is the Basic File and the other is the Contrast File. It can line out the different waveform segments of the basic file in the contrast file. Meanwhile, it can count the number of the difference.

# 4.9.1 Basic Software Setup of Data Contrast

STEP 1.Click Data on the Menu Bar, then selec	t 🞽 to open the Data Contrast Setting	s dialog box.
	Data Contrast Settings	×
	Active Data Contrast	
	Contrast Files	_
	Basic File 2.alc	-
	Contrast File 1.alc	-
	Contrast Beginning Point Error Tolerance	
	Contrast Result	Error Stat.
	A0[A0] FAIL	8
	A1[A1] PASS	
	A2[A2] PASS A3[A3] PASS	
	A4[A4] PASS	
<u>Data Tools Window Help</u>	A5[A5] PASS	
🔁 Select an Analytic Range	A6[A6] PASS	
noise Filter	Roll the contrast waveforms synchronization	
📩 Bus Width Filter	<ul> <li>Display files the contrast differences</li> </ul>	Pin Assignment
👱 Data Contrast	<ul> <li>Display files horizontal</li> </ul>	Perform Contrast
👪 Find Data Value Ctrl+F	🔽 Do contrast automatically when being run	
Find Pulse Width	Apply Close	Help

Fig4-153 - Data Contrast Interface

Activate Data Contrast: Click the checkbox to activate the function of Data Contrast.

Basic File: It is the standard contrast file.

Contrast File: It is used to compare with the Basic File.

Contrast Beginning Point: It can set the beginning point of the contrast at Trigger Bar or Beginning of Data.

Error Tolerance: It is the allowable time error when setting data contrast.

**Contrast Result:** It displays the same contrasted result and the different contrasted result with PASS and FAIL respectively.

Error Stat. : It displays the number of discrepant parts.

Pin Assignment: Users can select the contrastive channel.

Perform Contrast: It can activate the Contrast at once.

**Display files horizontal:** The waveform window of the two contrast files are displayed in horizontal. Users can select it as their requirements and the default is non-activated.

Roll the contrast waveforms synchronization: The two contrast files roll synchronously. Users can select it



as their requirements and the default is non-activated.

**Display files the contrast differences:** It can line out the difference in the contrast waveform. Users can select it as their requirements and the default is non-activated.

**Do Contrast automatically when being run:** The two files will be contrasted automatically when being run. **Tip:** For this function, Data Contrast, we provide the SDK Development Tool for users. Users can customize the Data Contrast Interface according to their requirements. We has packed the Data Contrast UI as the GUI.DLL and designed an interface which is used for the communication between the GUI.DLL and Main Program. The GUI adopts the Non-modal Interface design, which can make the GUI Interface and Main Program Interface switch freely. When users activate the Data Contrast function, the software will search whether there is a GUI. DLL or not, then it can judge whether there is a user-defined Interface. If there is a user-defined Interface, the GUI.DLL will take effect; if there isn't, the embedded Data Contrast Interface will be activated.

STEP 2. Display the contrast results in the Data Contrast dialog box.

**Tip**: After pressing Perform Contrast, it will display the contrast information in the contrast result. The below contents of the box are the contrast information. The information is relative simpleness; if users don't want to understand more details, you can know whether the signals of the two contrast files are completely the same or not.

Data Contrast Setting	gs			×
🔽 Active Data Contra	ast			
Contrast Files				
Basic File	:.alc		•	
Contrast File	.alc		•	
Contrast Beginning P	oint	Error Toleran	ce	
T Bar		None		-
C Beginning of Dal	ta	Intone		
Contrast Result			Error	Stat. 🔺
A0[A0] FA			8	
A1[A1] PA: A2[A2] PA:				
A3[A3] PA				
A4[A4] PA:				
A5[A5] PA: A6[A6] PA:				
Roll the contrast v	uqueforme el	Inchronization		
			Pin Ass	ignment
Display files the c		ences	Derform	n Contrast
Display files horizo	ontal		Ferrori	Contrast
🔽 Do contrast autor	matically whe	n being run		
	Apply	Clos	e	Help

Fig4-154 - Display the Contrast Results in the Data Contrast Settings Dialog Box **A0[A0]**.....**FAIL:** It indicates that there are differences in the channels of the two files. **B0[B0]**.....**PASS:** It indicates that there is no difference in the channels of the two files. STEP 3. Display the contrast results in the waveform windows. See the figure below.



**Tip**: It contrasts the two data files in the waveform area. The contrast waveform and the basic waveform are displayed horizontally; we can roll the mouse to contrast the waveform files; the difference of the waveforms will be lined out with the red wave line "~~~~~~" in the contrast files.

🐝 ZEROPLUS-LAP-C (32)	2000) Standau	ard V3.11(CN01) (S/N:000000-0000) - 1
		Data Jools Mindow Help
		📅 📲 🛐 🕨 🕪 🔲 2K 💌 🗤 🖓 100KHz 💌 🗤 🛲 50% 💌 💠 🆓 Page 1 💽 Count 1 🔍 着
	(*) III   III -	
<mark>≸ 1</mark> Scale:1.837051us		
Total:20.48ms		Display Pos:-227.693289us A Pos:-120us   ♥ A - T = 120us   ♥ A - B = 270us   ♥ Display Range:-273.619564us B Pos:150us   ♥ B - T = 150us   ♥ Compr-Rate:No
Bus/Signal	Trigger F	Filter 📕 🛛 – 264, 484 309-255, 249054-246, 063799-236, 878544-227, 693289-218, 508034-209, 322779-200, 137524-190, 952269-181, 72
🥑 AO AO		
🝼 A1 A1		
🥑 A2 A2		
🥑 A3 A3		
🥑 A4 A4		
✓ A5 A5		
<b>1</b>		
Scale: 1.837051us		Display Pos:-227.693289us A Pos:-150us - A - T = 150us - A - B = 300us -
Total:20.48ms	D	Display Range:-273.619564us B Pos:150us - B - T = 150us - Compr-Rate:1.000
Bus/Signal	Trigger F	Filter – -264. 434309-255. 249054-246. 068799-236. 878544-227. 693289-218. 508034-209. 322779-200. 187524-190. 952269-181. 7
🝼 AO AO		
✓ A1 A1		
🧹 A3 A3		
✓ A4 A4		
<b>~ A5</b> A5		
🥑 A6 A6		
•	• • •	
Roady		Endi DEMO

Fig4-155 - Display the Contrast Results in the Waveform Windows

### Tip:

The Data Contrast function is available for the LAP-321000U-A , LAP-322000U-A, LAP-C(162000), LAP-C(321000) and LAP-C(322000) Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A , LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(32128) Modules.



# 4.10 Refresh Protocol Analyzer

The Refresh Protocol Analyzer function enables the system to analyze the data between Ds and Dp again.

# 4.10.1 Basic Software Setup of Refresh Protocol Analyzer

STEP 1.Click **Tools** on the Menu Bar, then select 👱 or click 🚾 on the Tool Bar directly to refresh Protocol

Analyzer.

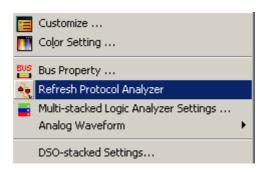


Fig4-156 - Refresh Protocol Analyzer

STEP 2. Transmit the tested Protocol Analyzer signal to the Logic Analyzer, for example Protocol Analyzer SPI.

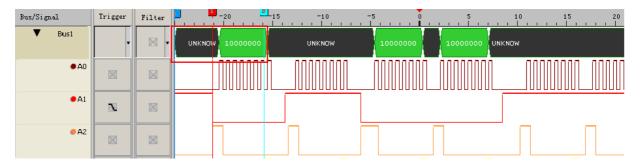


Fig4-157 - Waveform before Refreshing

STEP 3. Choose Select an Analytic Range to select the analysis range, and drag Ds Bar to B Bar.

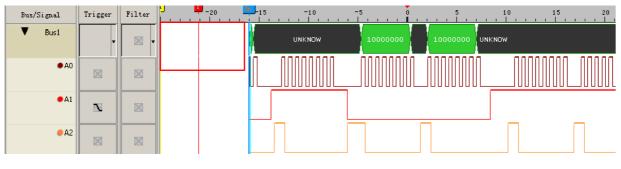


Fig4-158 - Drag Ds Bar to B Bar

STEP 4. Click s, the Logic Analyzer will analyze the data between Ds and Dp.



**4** 

Bus/Signal	Trigger	Filter	-20	15	-10	-5		5	10	15	20
▼ Bus1	•		ι	NKNO	w		10000000	10000000	UNKNOW		
• A0											
• A1	N										
● A2											

Fig4-159 - Analyze the Data Between Ds and Dp

STEP 5.Click 🔤 again, the waveform return the original state.									
Bus/Signal	Trigger	Filter		-20	5 -10	-5 0	5	10	15 20
▼ Bus1	•		UNKNOW	10000000	UNKNOW	10000000	10000000	UNKNOW	
• A0									
• A1	N								
<b>e</b> A2									

Fig4-160 - Restore the Original State

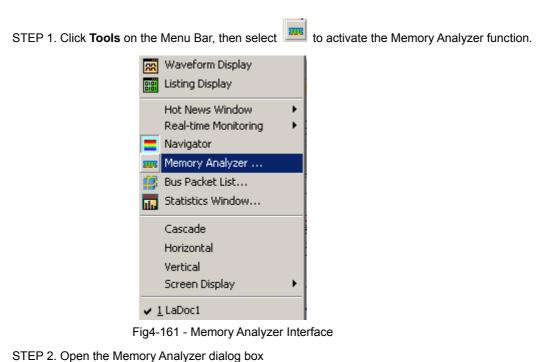
Tip: The Refresh Protocol Analyzer function can come into effect, while the Ds and Dp are activated.



# 4.11 Memory Analyzer

Memory Analyzer enables the system to divide the packet format in the Protocol Analyzer and display the Address and Data in an independent list. It is better for understanding the relative relationship and status of the Address and Data in the operating process of the Protocol Analyzer. Users will know the operation when they use this function. It improves the efficiency of knowing the conditions.

# 4.11.1 Basic Software Setup of Memory Analyzer



× 	<< < Bus1(I2C)		>> Op	tion I	import	Export	Merge	R	efresh	Reset	Display Al	teration		M				1
	Address	Write d	ata	Read data														-
		0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F	
								Uni	used:0X0	)~0X4F								
	0X50	0X00	0X79	0X89	OXAB	OXCD .	OXEE											
						- 🗸 C	ompact Mode	,Uni	used:0X6	)~0X7F								
						C	omplete Mode											
						_												
																		•
	•																	

Fig4-162 - Memory Analyzer Dialog Box

#### 1. Compact Mode and Complete Mode:

Click the Right Key in the memory analyzer dialog box; there are two modes for selecting, which are the Compact Mode and the Complete Mode. See the two different figures:



( 	<< <	>	>> Op!	tion	Import	Export	Merge	R	efresh	Reset	Display Al	eration		14				
	Bus1(I2C)																	
	Address	Write d	ata	Read data														74
		0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F	
								Uni	used:0X0	00~0X4F								
	0X50	0X00	0X79	0X89	OXAB	OXCD	OXEE											
						🗸 🗸 🗸	ompact Mod	e <u>I</u> Uni	used:0X6	60~0X7F								J
						Co	omplete Mod	le 🛛										
						_												
																		_
	4																•	•

Fig 4-163 - Compact Mode

×	<< < Bus1(I2C)	>	>> Optio	on	Import	Export	. Merge.		Refresh	Reset	Display Alte	eration		M			,	
		White o	data R	ead data	1													
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	
																.Unused:(	)XOO~OX4F	
	0X50	0X00	0X51	0X79	0X52	0X89	0X53	Cor	npact Mode	XCD	0X55	OXEF	0X56		0X57		0X58	
								🗸 Cor	nplete Mode							.Unused:(	)X60~0X7F	1
	4																Þ	

Fig 4-164 - Complete Mode

## 2. Buttons:

- : It is used to find the first packet.
- : It is used to find the previous packet.
- : It is used to find the next packet.
- >>>: It is used to find the last packet.

Option... : It is used to set the relative parameters for the List Window of the Memory Analyzer; see

the following Option dialog box:

Option			×
Bar Assignm	ent		
	Reaction Bar	A	•
Active Displa	y Assignment		
	Display Width	16	•
Color —			
Addr		Data(R)	
Data(W)		Alteration	
	OK	Cancel	Default



Reaction Bar: The default is the A Bar; the added Bar can be displayed and selected in the pull-down

② 孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

menu if users have added a new Bar. The data position of the Reaction Bar will be displayed in the List Window of the Memory Analyzer.

Note: The Ds/Dp Bar and T Bar can't be displayed in the pull-down menu.

**Display Width:** It is used to set the display width of the List Window of the Memory Analyzer; the default is 16. Users can select the 4, 8, 16 and 32 from the pull-down menu, and they also can input a value between 1 and 100.

**Color:** Users can vary the color of Addr, Data(R), Data(W) and Alteration as their requirements. The default color of the Addr is black; the default color of the Data(R) is blue; the default color of the Data(W) is red; and the default color of the Alteration is gray.

Import... and Export... : The Export function can select the TXT or EXCEL format to store the

Data of the List Window of the Memory Analyzer; the Import function also can select the TXT or EXCEL formats to analyze the former export data.

Merge...

: It can merge with the different export files. See the Merge dialog box below.

rge		
1	2	3
Object file:	C://10.txt	Open
File to merge;	C://11.txt	Open
	ОК	

Fig4-165 – Merge Dialog Box

#### **Object File:**

1. It is the covered file, that is to say, it is a new file.

- 2. It can display the path of the "Object File" and the file name.
- 3. It can open the "Object File" by clicking the "Open" option.

#### File to merge:

- 1. It can create the new file with the object file.
- 2. It can display the path of the "File to merge" and the file name.
- 3. It can open the "File to merge" by clicking the "Open" option.

#### Refresh

Pressing this button can refresh the data status of each Address data when there are

some alterations in the Bus Data

Reset

. The data status of each Address will be cleaned out and returned to the original status by

pressing the button.

Display Alteration

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

: The Data in the List Window of the Memory Analyzer will be cleared by pressing this

button and the List Window will display the alteration status of each cell. If the same Address has been written or read repetitively, the background of the cell will be gray and the list window will display the Data of the last packet. If the Address doesn't have any alteration, the Address Data will display the data of the Address without the background color. If it is the first time that the Address has been read, we confirm that the data of the packet has been altered.

: When users input the Address in this Edit Box and click the Find icon, it will go to the

corresponding position which is highlighted by the Blue frame.

STEP 3 .Display the Memory Analyzer function in the waveform window.

**Tip:** The Packet is read; the Address is 0X50; the Data are 0X00, 0X79 in sequence.

🐝 ZEROPLUS-LAP-C(32	128) Standa	rd ¥3.11(CN	N01) (5/N:000000-0	000) - [I2C]							_ 🗆 ×
🏂 Eile Bus/Signal Trigg	ger Run/ <u>S</u> top	p <u>D</u> ata <u>T</u> o	ools <u>W</u> indow <u>H</u> elp								_ 8 ×
🗋 😂 🔛 🎒 🕮	🕰 (ga 🚽	P 47 4	🔟 🕨 🕨	2K 💌 🛤	I 5MHz	<b>→ ハハ ハハ</b> 505	<b>% ▼ 👫 </b> ₽8	nge 1	- Coun	t 1	▼ 台
🖪 📰 🥵 🖌 🦌	👋 🗰 🛛	🚟 🔹 1.4	150216u: 🔻 🚢 🐴		e 🔐 👪 14	- 🖓 - 📴	🔶 Height	22 👻	Trigger De	lay 200i	ns
Scale:1.450216us			Pos:35.5303us	A Pos:-52			52.0884ms 💌		A - B = 6us		
Total:78.6034ms		Display F	Range:-725.108169	ns B Pos:-52	.0824ms 🔻	B - T =	52.0824ms 🔻		Compr-Rat	te:191.903	
Bus/Signal	Trigger	Filter	-20	-15	10 .	5	5	10	15	20	25
Bus1 (I2C)	-	⊗ -		DDRESS: 0X50	WriteA	-ACt	DATA: 0X00		D-AC DATA		
•A0 A0	x				\$1 2.21 2.21	2.212.212.212.	212.212.212us	1 2.2 1 2.2	1 2.2 1 2.2 1	2.212.21	2.21 2.2
●A1 A1		$\otimes$	2.2 3.2us3.2us3.2u	s		50.8us				9.6us	3.2us
		$\otimes$					78.603ms				
🥑 A3 A3		$\otimes$					78.603ms				
✓ A4 A4		$\otimes$					78.603ms				
🧹 A5 A5		$\otimes$					78.603ms				
🥑 A6 A6		$\otimes$					78.603ms				
✓ A7 A7		$\otimes$					78.603ms				
<b># BO</b> BO		$\otimes$					78.603ms				
🝼 B1 B1		$\otimes$					78.603ms				
		$\otimes$					78.603ms				
🥑 B3 B3		$\otimes$					78.603ms				
		$\otimes$					78.603ms				
✓ BS BS		■ ○					78.603ms				
×	>> Optio		oort Export	Merge R	efresh F	eset Display Alte		M			
Bus1(I2C)			Export	inorgani k		Cosec Dispidy Aice		<u>6*8</u>			
Address Data	ata Re Address	ead data Data A	ddress Data	Address Data	Address	Data Address	Data Addres	s Data	Address	Data A	dress
					1					.Unused:0XC	IO~OX4F
0X50 0X00	0X51	0X79	0X52 0X89	0X53 0XAB	0X54	OXCD 0X55	OXEF 0X56		0X57	Unused:0X6	DX58
										Onuseu.UAD	007/1
											<u> </u>
Ready									Endi	DEMC	

Fig4-167 – Memory Analyzer Display

# 4.12 Multi-stacked Logic Analyzer Settings

孕龍科技股份有限公司

roplus Technology Co., Ltd.

The function of the Multi-stacked Logic Analyzer Settings is mainly for connecting the hardware of many Logic Analyzers which are the same type, and then use the software to stack the Logic Analyzers which are working independently. It can improve the functions of the Logic Analyzer, which are mainly manifested in two aspects, expanding the RAM Size and adding the number of the test channels.

Tip:

1. The max. number of the Multi-stacked Logic Analyzers is four. The RAM Size of the four Logic Analyzers can reach to 128K\*4 and the test channels of the four Logic Analyzers can reach to 32\*4.

2. The function of the Multi-stacked Logic Analyzer Settings is available for the LAP-32128U-A, LAP-321000U-A, LAP-322000U-A, LAP-C(32128), LAP-C(321000) and LAP-C(322000) Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(162000) Modules.

## 4.12.1 Basic Software Setup of Multi-stacked Logic Analyzer Settings

STEP 1.Click **Tools** on the Menu Bar, then select **i** to activate the function of Multi-stacked Logic Analyzer Settings.

Customize Co <u>l</u> or Setting	
 Bus Property Refresh Protocol Analyzer Multi-stacked Logic Analyzer Settings Analog Waveform	•
DSO-stacked Settings	

Fig4-168 - Multi-stacked Logic Analyzer Settings Interface

STEP 2.Click 📕 to open Multi-stacked Logic Analyzer Settings dialog box.

Multi-stacked Logic Analyzer Settings
Activate Stack
Stack Type
Memory Stack
O Channel Stack
Please select the Logic Analyzer for stacking
M1 S/N:000000-0000
M2 S/N:000000-0000
□M3 S/N:000000-0000 □M4 S/N:000000-0000
M4 5/N:00000-0000
Synchronous Channel
AO
Synchronous Trigger Condition
Rising Edge
OK Cancel Help

Fig4-169 - Multi-stacked Logic Analyzer Settings Dialog Box

 孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

Activate Stack: Click the checkbox to activate the function of the Multi-stacked Logic Analyzer; the default is non-activated.

Stack Type: Users can select the Memory Stack and Channel Stack; the default is the Channel Stack.

**Please select the Logic Analyzer for stacking:** It can display all the connected Logic Analyzers and the S/N code of them. The M1 indicates the first Logic Analyzer and the M2 indicates the second Logic Analyzer; M3 and M4 are similar to the previous. Users should select two or more Logic Analyzers, but the most analyzers users can select is four.

**Synchronous Channel:** Select the synchronous channel form the pull-down menu. The default synchronous channel is A0.

**Synchronous Trigger Condition:** Select the synchronous trigger condition. Users can select the Rising Edge, Falling Edge, High and Low from the pull-down menu. The default is the Rising Edge. The function of the Synchronous Trigger Condition can only be used in the Channel Stack, that is to say, it is disabled in the Memory Stack.

STEP 3. Display the function of Multi-stacked Logic Analyzer in the Memory Stack.

**Tip:** There are two Logic Analyzers to do the Memory Stack; the Synchronous Channel is A0; the data on the left of A Bar is captured by the first Logic Analyzer, the data on the right of A Bar is captured by the second Logic Analyzer.

e 🖪 🥌 🌆	🛛 🖓 Tring 🛛 🖓		🔟 🕨 🕨 🗌 128K 💌 👬 👬 200MHz 💌 🚥 🚽 50% 💌 🎋 🆓 Page 1 🕑 Count 1 💌
📰 🥵 🖹	🖑 🛍 📗	× 0.	5812272! 🔽 💒 🎇 🚅 🎎 🔛 🔛 👹 14 🛛 🔯 🗸 💼 👓 Height 🛛 28 💌 Trigger Delay 🚺 10ns
e:10ns I:81.92us			yPos:0ns A Pos:+150ns ▼ A - T = 150ns ▼ A - B = 300ns ▼ yRange:-250ns ~ 280ns B Pos:150ns ▼ B - T = 150ns ▼ Compr-Rate:No
Bus/Signal	Trigger	Filter	▲ 62587.303 63447.552 64307.8 65168.049 66028.298 66888.547 67748.796 68609.045 69469.294 7
🝼 A0 (SYNC)	⊗ -	⊗ -	262144
🝼 A1 A1	Z	$\otimes$	1 490 490 489 490 489 491 460 516 978 980 981 980
🥑 A2 A2		$\otimes$	262144
🥑 A3 A3		$\otimes$	262144
🥑 A4 A4	$\square$	$\otimes$	262144
<b>45</b> A5		$\otimes$	262144
🍼 A6 A6	$\boxtimes$	$\otimes$	262144
<b>« A7</b> A7	X	$\otimes$	262144
<b>d BO</b> BO	$\boxtimes$	$\otimes$	. 262144
🍼 B1 B1		$\otimes$	262144
🍼 <b>B2</b> B2		$\otimes$	262144
🥑 B3 B3		$\otimes$	262144
🥑 B4 B4		$\otimes$	262144

STEP 4. Display the function of Multi-stacked Logic Analyzer in the Channel Stack.

**Tip:** There are two Logic Analyzers for Channel Stack; the Synchronous Channel is A0; the Synchronous Trigger Condition is the Rising Edge; the former 32 channels (A0~A7, B0~B7, C0~C7, D0~D7) change into the 64 channels (A0~A7, B0~B7, C0~C7, D0~D7, E0~E7, F0~F7, H0~H7, I0~I7) channels.



🂪 Eile Bus/Signal Trigg		Data Too		▼ mu = 50% ▼ 🖗 🐝 Page 1	×□_ ×8_
			128K ▼ ₩ ₩ 200MHz 812272!▼ ≝ ₩ ₩ ₩ ₩ ₩ ₩ ₩		rigger Delay 10ns
Scale:10ns Total:81.92us		Display P		A - T = 150ns ▼ B - T = 150ns ▼	A - B = 300ns I▼ Compr-Rate:No
Bus/Signal	Trigger	Filter	-7599.088 -5214.318 -2829.548 -444.	778 1939.991 4324.761 6709.531	9094.301 11479.071 138
🖌 A0 (SYNC)		× 🔍	54658		
🝼 A1 A1		$\otimes$	56129	1960 1959 1962 19	57 1963 1957 19
✓ A2 A2	$\boxtimes$	$\otimes$		120195	
🥑 A3 A3		$\otimes$		120195	
✓ A4 A4	$\boxtimes$	$\otimes$		120195	
<b>4</b> 5 A5		$\otimes$		120195	
<b>46</b> A6		$\otimes$		120195	
<b># A7</b> A7		8		120195	
<b># BO</b> BO	$\boxtimes$	$\otimes$		120195	
<b># B1</b> B1		$\otimes$		120195	
<b>€ B2</b> B2		$\otimes$		120195	
🥑 <b>B3</b> B3		$\otimes$		120195	
<b>d</b> B4 B4	$\boxtimes$	$\otimes$		120195	
		<b>D</b> I			v V

# 4.13 DSO-stacked Settings

To use the DSO-stacked function between Logic Analyzer and DSO, it is necessary to install specialized software to connect if using the DSOs produced by other manufactures except our company.

To use the Tektronix DSOs to stack, please download the <u>TEKVISA CONNECTIVITY SOFTWARE</u> <u>V3.3.4</u> version or higher from the Tektronix Website.

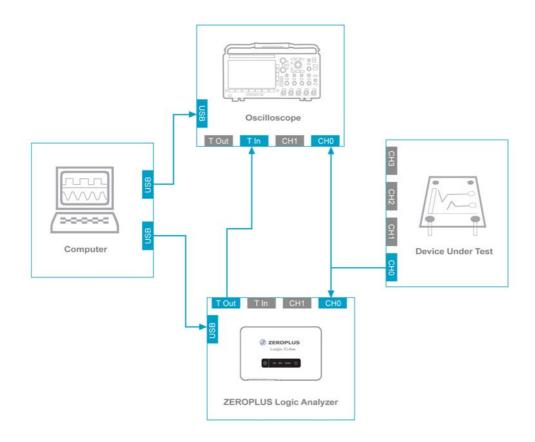
## Supported DSO Model:

DSO Manufacture	Model	On-line Mode	
Tektronix	TDS1000 Series	USB	
	TDS2000 Series	USB	
	TDS5000 Series	GPIB	Logic Analyzer software
			will be installed in the
			system of 5000 series.

## **Operating Mode**

(1) Host-Slave

LA is the Host, DSO is the Slave. Connect the Trigger Out of LA with the Trigger In of DSO, when LA has been triggered, it will inform DSO to capture signal.

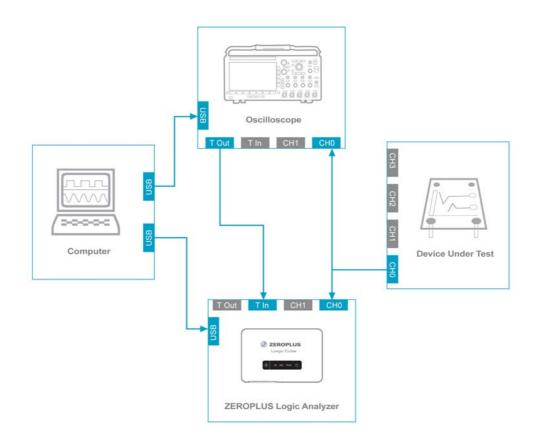


## (2) Slave-Host

a) DSO is the Host, LA is the Slave. Connect the Trigger Out of DSO with the Trigger In of LA, and the LA uses external trigger. When DSO has been triggered, it will inform LA to capture signal.(LAP-B Series support)

b) DSO is the Host, LA is the Slave. Connect the Trigger Out of DSO with any channel of LA(users can define),
 which occupies one channel. When DSO has been triggered, it will inform LA to capture signal. (LAP-C series
 V3.11 higher version support)

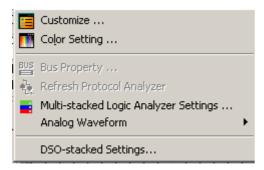




## **Operating Instructions**

STEP 1. Confirm the DSO is connected correctly.

STEP 2. Click the Tool on the Menu Bar, than select DSO-stacked Settings to open the dialogue box.





STEP 3. Set the Channel V/Div in the dialogue box.

D!	50-stacked Settin	ıs			×
	-Channel V/Div Setti	ig			_
(	DSO_CH1 V/Div:	2V/Div 🔽 DSC	_CH2 V/Div:	2V/Div 💌	Ŋ
	DSO_CH3 V/Div:	2V/Div 💌 DSC	)_CH4 V/Div:	2V/Div	IJ
	-Channel Setting				
	🔲 Only display DS	0			
	DSO_CH1	🗆 DSO_CH2 🛛 🗖 DSC	р_снз 🗖	DSO_CH4	
			•••	•••	
	-Channel Height Set	ing			
	DSO_CH1 Height:	80 DSO_	CH2 Height:	80	
	DSO_CH3 Height:	80 DSO_	CH4 Height:	80	
	DSO Settings	OK Cancel	Defau	t Help	

STEP 4. Set the Channel Waveform Color and select the DSO Channel to be displayed on LA software.

DSO-stacked Settings
Channel V/Div Setting
DSO_CH1 V/Div: 2V/Div  DSO_CH2 V/Div: 2V/Div
DSO_CH3 V/Div: 2V/Div  DSO_CH4 V/Div: 2V/Div
Channel Setting
C Only display DSO
DSO_CHI DSO_CH2 DSO_CH3 DSO_CH4
Channel Height Setting
DSO_CH1 Height: 80 DSO_CH2 Height: 80
DSO_CH3 Height: 80 DSO_CH4 Height: 80
DSO Settings OK Cancel Default Help



STEP 5. Select the Only display DSO according to users requirements.

D	50-stacked Settings
	Channel V/Div Setting
	DSO_CH1 V/Div: 2V/Div  DSO_CH2 V/Div: 2V/Div
	DSO_CH3 V/Div: 2V/Div  DSO_CH4 V/Div: 2V/Div
	Channel Setting
ſ	Conty display DSO
	🔽 DSO_CH1 🔽 DSO_CH2 🗌 DSO_CH3 🔲 DSO_CH4
	Channel Height Setting
	DSO_CH1 Height: 80 DSO_CH2 Height: 80
	DSO_CH3 Height: 80 DSO_CH4 Height: 80
	DSO Settings OK Cancel Default Help

STEP 6. Set the Channel Height.

DSO-stacked Settings	×
Channel V/Div Setting DSO_CH1 V/Div: 2V/Div  DSO_CH2 V/Div: 2V/Div DSO_CH3 V/Div: 2V/Div DSO_CH4 V/Div: 2V/Div	
Channel Setting Only display DSO DSO_CH1 DSO_CH2 DSO_CH3 DSO_CH4	
Channel Height Setting	1
DSO_CH1 Height: 80 DSO_CH2 Height: 80 DSO_CH3 Height: 80 DSO_CH4 Height: 80	
DSO Settings OK Cancel Default Help	



STEP 7. Press the DSO Settings button to open the dialogue box.

D	50-stacked Settin	gs		×
	-Channel V/Div Setti	ng		
	DSO_CH1 V/Div:	2V/Div	DSO_CH2 V/Div:	2V/Div 💌
	DSO_CH3 V/Div:	2V/Div	DSO_CH4 V/Div:	2V/Div
	-Channel Setting			
	🔲 Only display D	50		
	DSO_CH1	DSO_CH2	🗆 DSO_CH3 🛛 🗖	DSO_CH4
	•••		•••	
	-Channel Height Set	ting		
	DSO_CH1 Height:	80	DSO_CH2 Height:	80
	DSO_CH3 Height:	80	DSO_CH4 Height:	80
	DSO Settings	ок	Cancel	lt Help

STEP 8. Select the connected DSO Manufacturer.( Currently it only supports Tektronix Manufacturer.)

0 Settings		2
Oscilloscope Brand:	Tektronix	•
Online Mode		
USB	C TCP/IP	O AUTO
IP:		1
Stack Parameters		
Current Online Model:		
🔲 Sampling Frequency:		Hz
🔲 Stacking Delay:		Ps
Trigger Position:		%
Trigger Channel:		V
Trigger Type		
🗖 Activate		
C Trigger Edge	<b>T</b>	
C Video	<b>_</b>	
C Pulse	<b>_</b>	ns

STEP 9. Set the Connection Mode to USB or TCP/IP according to the connection mode of DSO. If selecting TCP/IP, it is necessary to key in the IP Address of current computer. Users also can select AUTO to auto-recognize the Online Mode.(Tektronix 1000,2000 series adopt the USB Interface to connect.)



SO Settings			×
Oscilloscope Brand:	Tektronix	-	
Online Mode			
USB	C TCP/IP	O AUTO	
IP:		]	
Stack Parameters			
Current Online Model:			
Sampling Frequency		Hz	
🔲 Stacking Delay:		Ps	
Trigger Position:		%	
Trigger Channel:	<b>V</b>		۷
Trigger Type			
🗖 Activate			
🔿 Trigger Edge	<b>_</b>		
C Video	<b>_</b>		
C Pulse	<b>V</b>		ns
		_	
Online	OK OK		Iancel

STEP 10. It will display the currently connected DSO Model after pressing the Online button.

DSO Settings		×
Oscilloscope Brand:	Fektronix	<u>~</u>
Online Mode		
USB	○ TCP/IP	C AUTO
IP:		]
Stack Parameters		
Current Online Model:	TDS 1002B-SC	
Sampling Frequency:	100000.00	Hz
🗖 Stacking Delay:	0	Ps
Trigger Position:	50	%
Trigger Channel:	External	1.00 V
Trigger Type		
C Activate		
Trigger Edge	Rising Edge 💌	
C Video	All Lines 🗾 💌	
C Pulse	<	100 ns
Disconnect	] ок	Cancel

STEP 11. Set the relevant parameter and press the OK button.

DSO Settings			X
Oscilloscope Brand:	Fektronix	7	
Online Mode			
USB	C TCP/IP	O AUTO	
IP:		]	
Stack Parameters			
Current Online Model:	TDS 1002B-SC		
Sampling Frequency:	100000.00	Hz	
🔽 Stacking Delay:	0	Ps	
Trigger Position:	50	%	
✓ Trigger Channel:	External	1.00	V
Trigger Type	Rising Edge		
C Video	All Lines		
C Pulse		100	ns
Disconnect	ок	Can	cel

STEP 12. Select DSO\_CH1 and DSO-CH2 channels to analyzer A0, A1 channels of LA. Below is the waveform it captured.

File Bus/Signal	• 🗷 🖗 🚽	<b>₩</b> , *B	8 0 00	2K 💌 🗟 👬		u mm 50% 👤	Ka⊨ a∳ Page Height 28		▼ A A Ø	8.8	_8
Scale:416.667KHz	S 🖑 🖬 🛛	💥 - 2.4u	Display Pos:Ons	Bar Bar Bar Bar	A Pos:-1		Height 28	▼ Trigger De A - T = 59.524KHz ▼		12 - B = 25.62KHz -	•
Total:204.8us			Display Range:-6	0us ~ 60.2us	B Pos:22	231579us   -		B - T = 44.981KHz -		Compr-Rate:No	
Bus/Signal	Trigger	Filter	-48us	-36us	-24us		Ons	12us	24us 36us	48us	60us
		8V 4V-									2V/Div
DSO_CH1		01						p			
		-4V- -8V									
		8V_ 4V-						ليستر فسنر لت		<b>F</b>	2V/Dix
DSO_CH2		00-					l \l		┝─┘└──┡┯┘		
		-4V- -8V									
🥑 AO AO	-	- X					nknown				
🥑 A1 A1							nknown				
🥑 A2 A2							nknown				
🧹 A3 A3							nknown				
🥑 A4 A4							nknown				
🥑 A5 A5		$\boxtimes$					nknown				
🥑 A6 A6		$\boxtimes$					nknown				
		$\square$				U:	nknown				
<b># BO</b> BO						U;	nknown				
<b>d B1</b> B1						U:	nknown				
<b>€ 82</b> 82		X				U	nknown				
🥑 B3 B3		×				U	nknown				
🥑 B4 B4						U:	nknown				
	• • • •										F
					<u>A</u>			B			



# **5** Troubleshooting

- 5.1 Installation Troubleshooting
- 5.2 Software Troubleshooting
- 5.3 Hardware Troubleshooting



# Objective

In this chapter, troubleshooting is divided into installation, software and hardware issues. These troubleshooting questions and answers depend not only on our engineers, but also on end users such as students, engineers, technical manual writers, and others.

# 5.1 Installation Troubleshooting

- Q1. Why it is not prompt when I insert the driver CD into my CD-ROM?
- A: At this stage, the driver CD is not auto-executable. The primary issue here is a chipset problem. Though these six Logic Analyzer models seem only different in model number, they are quite different in firmware and chipsets. Due to installation procedures (see *Chapter 2*), we are unable to compile a driver program that auto-detects the chipset at the beginning of the installation.
- Q2. Why does the installation software keep giving an error message saying that I don't have enough memory?
- A: This kind of problem happens in many hardware installations. Turn off multimedia programs such as Media Player, media decoders, media encoders, and so on. If there are any multimedia icons in the system tray (see the far right end of the **START** menu taskbar), remove them. The Logic Analyzer software will run better in memory locations from 64 to 512 MB.
- Q3. What should I do if I want to share this software interface with all users of my computer after installing it?
- A: The shortcut is removing the software interface, and then reinstalling it. By default, the program is available for all users.

#### Q4. My HDD is modest; which software components are absolutely necessary?

A: Choose **Custom** as your setup type. Next, unselect items such as examples and tutorials. You must install at least the Main App (application).

#### Q5. My MS Windows system will not accept the driver; what should I do?

A: Double check that you run the correct Setup.exe from the folder that corresponds to your hardware and MS Windows version. Visit our website for the latest updated or debugged software. If you are running this program on a virtual machine, the virtual machine may not support the amount of hardware addressing. In this case, try it with a machine that is physically running a Windows system.



# 5.2 Software Troubleshooting

#### Q1. Can I run the program even if I don't have the Logic Analyzer hardware?

A: Yes, you can. You can run the program under the demo mode. See. Fig5-1.

隊 ZEROPLUS Logic Analyzer	×
Hardware Searching failed!	
Run Demo Retry Exit	

Fig. 5-1: Select **Run Demo** if you do not have the actual hardware.

- Q2. I am running a graphing program and software at the same time. Whenever I try to make a screenshot of my work, it keeps telling me that I have insufficient memory space; what is wrong?
- A: A few users have reported similar problems. We are not certain what causes it or how to fix it. However, we have found that if there is a defective address within 128 MB to 512 MB in your physical memory, your software might signal "End of memory". Thus, the program will warn you about insufficient memory. Test your memory with a varied memory testing program. Or, take a screenshot, close the program, paste it to the graphing program, and re-open the program.
- Q3. A part of the background picture remains within the Waveform Display Area, especially when running the program in demo mode. What's wrong with it?
- A: Your machine may have a memory management problem with either your physical RAM onboard or the RAM on your video card. Turn off any other multimedia of graphic programs and then re-run the software. If this does not work, restart your system. This should temporarily fix the problem. However, we highly recommend terminating all irrelevant programs while working with the Logic Analyzer (Try not to burn DVDs, not listen to music or watch movies while working with the Logic Analyzer.).
- Q4. The default color setting of the Waveform Display Area is very cool, but I don't see anything when I print my work out with my black and white laser printer. What can I do?
- A: Refer to Section 3.6; it should have clear, understandable instructions about changing the color of the user interface. See *Fig. 3-153*; this color setting should give a clear view of the Waveform Display Area, even with an old black and white laser printer.



# 5.3 Hardware Troubleshooting

## Q1. Why are no lights on when I hook the USB cable to the Logic Analyzer?

A: Double check whether the other end is properly connected to your PC. There may also be a defect in your USB cable. Try another cable.

## Q2. Why can't I read any signals from my Logic Analyzer?

A: Check whether you have correctly connected the signal cables to the activated pin on your test board and check the power supply of your test board. The Logic Analyzer does not supply any electricity to a test board via signal lines.

#### Q3. I get a signal from only one Logic Analyzer when I have two connected; what is wrong?

A: Currently, only the LAP-32128U-A, LAP-321000U-A, LAP-322000U-A, LAP-C(32128), LAP-C(321000) and LAP-C(322000) support many Logic Analyzers working in series. Also, make sure that the signal lines, power lines, and ground line are properly connected. Refer to Fig. *1-11, Table 1-2, Table 1-3, Table 1-4*, and *Table 1-5*.

## Q4. Why should I bother grounding? Where can I ground?

A: Grounding will protect the Logic Analyzer and the test board. A proper ground may improve the quality and accuracy of your data. Since it is impossible to avoid unwanted interference you may ground the Logic Analyzer with the test board to ensure that unwanted interference will equally disturb both the testing and tested devices, ensuring a set of data that is still accurate.

# Conclusion

Every user of a product is a potential writer for *Chapters* 5~7 in this User Manual. In fact, this chapter is a composition of many unnamed electronic professionals, especially experts.



- 6.1 Hardware
- 6.2 Software
- 6.3 Registration
- 6.4 Technical Information
- 6.5 Others



# Objective

In this chapter, common problems and questions are roughly classified into five categories: Hardware, Software, Registration, Technical Information, and Others. This is a backup resource for users, especially those without Internet access. Most references refer to English web links.

# 6.1 Hardware

#### H01. Is it ok to substitute stock items for bundled cables and connectors?

A: Yes, users may use any compatible connectors and cables. However, to ensure consistency and accuracy in measurements and data, we strongly recommend using the bundled connectors and cables. Each of the Logic Analyzer's is calibrated with the bundled cables and connectors before packing.

## H02. Does Zeroplus manufacture grippers? How may I purchase grippers?

A: Yes, we have a production line dedicated to grippers. Contact our sales department and a sales representative will be happy to assist you.

#### H03. Is the memory size fixed? If I just use one of the ports, can I expand the memory size?

A: The Logic Analyzer's memory is fixed at 4 megabits. Due to current hardware limitations, the memory size cannot be modified, even as the number of ports used changes.

## H04. Are different external sampling frequencies for different channels possible?

- A: No, there is only one external sampling frequency available.
- H05. Can I disable or set a certain port to don't care while during compression?
- A: No, during compression, D Port will be set to be **disabled**.

#### H06. Why does the Logic Analyzer feature negative voltage calibration?

A: This allows users to analyze any given signal.

#### H07. How do I adjust the Trigger Level?

A: The adjustment of the trigger level is done with a port which consists of 8 channels. The trigger lever can only be adjusted for an entire port.

#### H08. Does the Logic Analyzer use hardware or software compression technology?

A: For time efficiency, the Logic Analyzer uses hardware compression.

#### H09. Is planning an Analyzer that can handle more channels?

- A: Yes, we are working in this direction.
- H10. Does the memory page vary when the depth of the memory changes?
- A: Yes, the depth of memory changes the memory page.

## H11. Is the Logic Analyzer expandable? How may I expand it?

A: Yes, the Logic Analyzer is expandable. At this stage, you can expand it with external module devices.

#### H12. Why must I reinstall the driver every time I use a different Logic Analyzer?

A: Since each Logic Analyzer has unique serial numbers, you must reinstall the driver every time you change the Logic Analyzer.

#### H13. Why is there no data? Why does data sampling seem inconsistent?

- A: The reasons are varied, but you may follow this checklist for troubleshooting:
  - 1) Always check the USB connection between the Logic Analyzer and your PC.
  - 2) We strongly recommend using USB ports in the rear panel of a PC; these ports usually have better voltage stabilities than front panel ports. However, if front panel USB ports are directly soldered to the main board, you can use them.
  - 3) Make sure the Logic Analyzer is directly connected with the PC (without a USB hub).
  - 4) Inconsistent data display may indicate voltage irregularities in the main board; examine capacitors on your main board or power supply.



5) If the problem is the power supply, we strongly recommend purchasing a power supply with a hardwired voltage transformer rather than a voltage regulator. For power supplies with the same output power, those built with hardwired voltage transformers are usually much heavier than those relying on voltage regulators.

## H14. What are the time settings for "Setup" and "Hold"?

A: Setup Time: 0.05ns ~ 0.25ns; Hold Time: 0.02ns ~ 0.08ns.
 Clock High requires a minimum of 0.31ns. Clock Low requires at least 0.47ns.



# 6.2 Software

#### SW01. Why is the compression function not enabled by default?

A: Mostly to avoid significant errors when testing signals with high variability, or measuring a certain channel for a long time period.

#### SW02. What is the purpose of the compression function?

A: The compression function measures signals that vary slightly over a long period.

#### SW03. Can I enable Trigger Page and Compression Function simultaneously?

A: Yes, you can.

#### SW04. When should I use the "Bar" function?

A: This function allows you to highlight a segment of a waveform so that you can have a closer view. Depending on the configuration of **Waveform Display Mode** under **Tools** → **Customize**, a more accurate numeric value of sampling site, time, or frequency difference will be calculated and displayed as shown in *Fig. 6-1*.

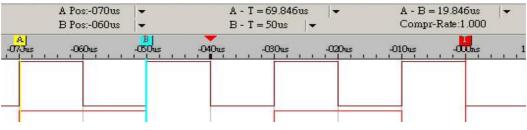


Fig. 6-1 – Bar Function

#### SW05. Can triggers be differentiated in Pre-Trigger and Post-Trigger?

A: Yes, they can.

#### SW06. Are all setup parameters and configurations saved as I save my work?

- A: Yes, everything in your work space, except signal graph, will be saved.
- SW07. If I have the wheel feature with my mouse (or other pointing devices), may I adjust the waveform display zoom, in the Waveform Display Mode by scrolling?
- A: This feature has been enhanced since V1.03. If your program version is prior to this version, visit our website for the latest update at

http://www.zeroplus.com.tw/logic-analyzer en/technical support.php

#### SW08. What are the extremes for Delay Time and Clock & Trigger Delay Clock?

A: The interface will inform you of the interval you may use. However, it varies from case to case, depending on your test devices. See *Fig.* 6-2.

Delay Time and Clock     Trigger Delay Time
5ns
(Min:5ns , Max:83.880955ms)
Trigger Delay Clock
1
(Min:1,Max:16776191)

Fig. 6-2 - Delay Time and Clock

#### SW09. How do I know the version number of my software interface program?

A: Click Help from the menu (See Fig 6-3), and then select About ZEROPLUS Logic Analyzer(See Figs 6-3 and 6-4).

X



Abo

	Logic Analyzer Help	F1				
	Keyboard Map					
	Problem Feedback					
	💡 About ZEROPLUS Log	gic Analyzer				
	About ZEROPLUS More Protocol Analyzer					
Fig. 6-3 – About ZEROPLUS Logic Analyzer						
at ZEB	OPLUS Logic Analyzer					
		LAP-A & LAP-C Series				
9	孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.	Version : Standard V3.11(CN01) S/N:000000-0000				

孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.         LAP-A & LAP-C Series           Version : Standard V3.11(CN01)         S/N:000000-0000
The Information of the Version
ZEROPLUS
LAP-C Series Standard V3.11
Welcome to use ZEROPLUS Logic Analyzer.
The document includes the version information
of the software.
Detailed description invites reference company website
Copyright(C) 1997-2011 ZEROPLUS TECHNOLOGY CO., LTD. Website: http://www.zeroplus.com.tw

Fig. 6-4 - The circled information is the version number.

## SW10. How may I upgrade my software interface program?

A: Visit our website at <a href="http://www.zeroplus.com.tw">http://www.zeroplus.com.tw</a> and follow the instructions for the English version. You may also use the following address for English updates. <a href="http://www.zeroplus.com.tw/logic-analyzer">http://www.zeroplus.com.tw/logic-analyzer</a> en/technical support.php

#### SW11. Can I save my signal data to a separate pure text file (\*.txt)?

A: This feature is available in this version.

#### SW12. Why is the text display covered by other text or outside the display width?

A: At this stage, our software interface program has missing code for multilingual support. You will have to ensure your system default encoding is one of the following languages: 1) any English Encoding (en, en-XX), 2) Traditional Chinese (zh, zh-XX), 3) Simplified Chinese (zh, zh-CN in HZ, GB2312, GB18030). Double check the language configuration in **Regional and Language Options**.



Fig.6-5 – Windows Regional and Language Options

SW13. Is there a Reset that restores the default color settings for signal output waveforms in the Position Signal Display Area?



A: Yes, there is. Click **Tools** from the menu bar, and select **Color Setting**; click **Defaults**. However, this restores everything in this window. You must make a further adjustment if the color setting is the only thing you want to restore. See *Fig. 6-6*.

Color Setting			×
Workaround Waveform	1		
Name	🔲 Relating	Color	
Waveform Background List Background 1 List Background 2 Cursor Grid Unknown Line Default Bus Bus Text List Text List Text Time Text Bus Error			
Bus Error Text Signal Filter Bar			
Preview 0 1 0 10 10	0 0 0	💶 🔲 automatical	esponding color
		When being background	g printed, the I is white.
40	Can	cel Default	Help

Fig. 6-6 - Restore Color Defaults

## SW14. Can I change the displayed waveform mode?

- A: Yes, you can. There are two ways to do this.
  - First, go through Data → Waveform Mode and choose a waveform. See Fig. 6-7.

	Select an Analytic Rang	ge	
<u>aaa</u>	Noise Filter		
ż	Bus Width Filter		
Ŧ	Data Contrast		
商	Find Data Value	Ctrl+F	
		CULU	
<b>F</b>	Find Pulse Width		
l <b>4</b>	To the Previous Edge	F11	
\$[	To the Next Edge	F12	
	Go To	+	
<b>+</b> 2 Ba⊦	Add Bar	Alt+A	
	Delete Bar	Alt+B	
N	Zoom	E	
8m	Hand	н	
R	Normal	ESCAPE	
ᇞ	Zoom In	F9	
K	Zoom Out	<b>F</b> 8	
	Show all Data	<b>F</b> 10	
K)	Previous Zoom	Ctrl+Z	
	Data Format	•	
	Waveform Mode	•	
	List Data Mode	•	

Fig. 6-7 - Waveform Mode

The second alternative is to right-click any place in the Waveform Display Area. Then, a menu will pop up. Click **Waveform Mode**, and choose a waveform. *See Fig. 6-8.* 



88	Find Data Value	Ctrl+F		
	Find Pulse Width			
	Go To	•		
	Place	•		
Bar	Add Bar			
	Zoom	E		
m	Hand	н		
R	Normal	ESCAPE		
2222	Show all Data	F10	1	
ก	Previous Zoom	Ctrl+Z		
	Data Format	•		
	Waveform Mode	Þ	~	Square Waveform
	Color		_	Sawtooth Waveform
	Bus Data Color			
	Bus Single Data Color		ι.	

Fig.6-8 – Waveform Mode

## SW15. Can I change the Signal Display Mode into the Timing Mode?

A: Yes, you can.

## SW16. Why does not Filter Delay work when the Double Mode is enabled?

A: To optimize signal output quality and maximize memory efficiency, the **Signal Filter Setup** function may work under the Double Mode. However, the **Filter Delay** function doesn't work under the Double Mode at this stage.



# 6.3 Registration

#### RG01. What is the significance of the hardware serial number?

A: Every product is assigned and engraved with a unique serial number, which allows us to trace the original manufacturing date of a specific product.

#### RG02. How do I register online?

A: Visit our homepage at <a href="http://www.zeroplus.com.tw">http://www.zeroplus.com.tw</a>. Choose the Instrument Department, and click on English. Once you finish membership registration, proceeding with product registration. After finishing product registration, you will receive an email consisting of your product registration information. A password may be required for further customer services and other inquiries.

#### RG03. What should I do if online registration fails?

A: Do a screen grab of the window, including the error message, and email our customer service dept. A customer service representative will be glad to assist you as soon as possible once the email is correctly received.

#### RG04. How may I register if the purchasing date was more than one month ago?

A: In this case, fill in the registration card and send it via post, fax, or email to our customer service dept, and a representative will process the registration for you.

#### RG05. What is the warranty length for my product?

A: A two-year FACTORY WARRANTY is offered in which you will have to send the defective product to the closest branch, an authorized service site, or our headquarters. The in-store warranty may vary, and many require extra charges for various extended warranty policies. The company is not being responsible for an in-store warranty that exceeds our factory warranty.

#### RG06. Why should I register this product?

A: If you do not register this product, the warranty will be counted from the manufacturing date indicated by the serial number of your product. Thus, we strongly recommend registering your product for your own benefit.

#### RG07. What should I do if the hardware serial number is previously registered?

A: In this case, take a picture of the decal on the rear side of the product and fill in the registration form. Call us and mail both picture and registration to us. A customer representative will be happy to assist you.

#### RG08. How do I register the protocol analyzer and buy protocols?

A: Every product is assigned and engraved with a unique serial number. please print your S/N number window as an example attachment and send it to our distributor or ZEROPLUS head office. According to your S/N, we will provide passwords for your protocol registration.



# 6.4 Technical Information

#### TI01. What is the Logic Analyzer?

A: The Logic Analyzer is a tool that sieves out and shows the digital signal from test equipment by using a clock pulse. The Logic Analyzer is like a digital oscilloscope. However, it only shows two voltage states (the logic status 1 and 0), differing from many voltage levels of an oscilloscope. The Analyzer has more channels than an oscilloscope to analyze the waveform. Since the Logic Analyzers obtains only signals 1 and 0, its sampling frequency is slower than an oscilloscope, which needs many voltage ranks. Moreover, the Logic Analyzer can receive many signals during a test.

#### TI02. How does the Logic Analyzer operate?

A: The Logic Analyzer reserves trigger requirement setting for users and uses them on the test equipment for the value of the sampling signals and puts them into the internal memory. The software of the Logic Analyzer will read out the value from the memory and switch it to the waveform or status shown for users' analysis.

## TI03. What is the asynchronous Timing Mode?

A: Since the sampling clock and tested objects are not directly related to each other, and the former won't be controlled by the latter, the sampling clock and the tested signals will not be done at the same time. We call this "Timing Mode", which means that in the same time interval, you can get sampling data from the test equipment at one time, such as every 10 seconds. The internal clock, the Logic Analyzer's inner confirmed one, is often for sampling in Timing Mode as is the logic waveform.

## TI04. What is the synchronous State Mode?

A: Because the sampling clock and measured object can be directly related, and are controlled by the latter, signals of the former and the latter can proceed simultaneously. We call this "State Mode". In this mode, the measured object provides the sampling clock. State Mode is when the Logic Analyzer can obtain sampling data from the test equipment synchronously. In other words, when the test equipment has a signal or signal group, this is the time to get the signal. For example, while the test equipment is sending out one rising edge, the Logic Analyzer can start to obtain one signal.

#### TI05. What are A-bar, B-bar and T-bar?

A: The T-bar, A-bar and B-bar are labels. T is the trigger label, which cannot be removed when the waveform or the state is displayed, which marks a pod. When searching for, or obtaining data, the A and B labels can be set in any location. Using the order of these markings, you can return quickly to the desired position to analyze data. This can also be a point to measure the interval between A-B, A-T, or B-T.

#### TI06. What is a Trigger Gripper?

**A:** A gripper is the gathering point to collect the Logic Analyzer channels. When a cable connector is not suitable for the test device, a trigger gripper may be an alternative for connection.

#### TI07. What is a Channel?

- A: The channel is the collection line of the input signal. Each channel is responsible for linking the pin of the measured device. Every channel is used to collect signals from the test equipment.
- TI08. How can I display acquisition in the waveform captured by external sampling signal?
- A: Select Waveform Display from the Window list.

#### TI09. What is an External Trigger?

A: An external trigger is a signal outside the Logic Analyzer. It is used for the simultaneous test of 2 test tools. For example, one Logic Analyzer can be started by one signal from another test tool. Or when it is triggered, it can output one signal to another test tool. The Logic Analyzer is often used for triggering an oscilloscope.

#### TI10. Why does Double Mode not coincide with Filter Delay?

A: In order to set out the perfect waveform from the Logic Analyzer and achieve optimal memory efficiency, you can use the **Signal Filter** when using **Double Mode**; the system doesn't support the function of **Filter Delay**.

## TI11. How do I update software?

A: The software will automatically check for and download updates. This function deletes old software first and then downloads and installs the latest version.



# 6.5 Others

#### OT01. How was the Logic Analyzer developed?

A: It took us more than two years to develop this product. We envision "Everyone carrying the Logic Analyzer," and we would like to make some contributions to the electronics industry in return. We also wish to transform the stereotypical OEM factory into a world class R&D center.

#### OT02. Why is there a rich information database for game chips rather than the Logic Analyzer?

A: First of all, we apologize for any inconvenience caused by the lack of information pertaining to Logic Analyzers. We are currently working very hard on multilingual information and documentations pertaining to the Logic Analyzer. Visit our website for the latest drivers, software, and manuals: <a href="http://www.zeroplus.com.tw/logic-analyzer\_en/technical\_support.php">http://www.zeroplus.com.tw/logic-analyzer\_en/technical\_support.php</a>. In the meantime, we will have updates ready when verified error free.

#### OT03. What was the original intention of developing this item?

A: Originally, the Logic Analyzer was just for use by our engineering department. Later on, we saw the greater need for this kind of device. We made numerous enhancements and made it available to the public.

# Conclusion

This chapter is full of hard facts for engineers. The contents of this version of the User Manual may look more different than the one on the web. Every engineer finds new problems, new solutions, or other issues, during real life applications. Though there are dozens of questions here, we look forward to your feedback, which is important for future versions. It may help us produce more efficient and accurate devices so that we will offer you much better service.



# 7 Appendix

- 7.1 Hot Keys
- 7.2 Contact Us



# Objective

In this chapter, users will learn the functions of all defined hot keys in the software interface of the Logic Analyzer.

Table 7-1: Hot Keys (1)

Hot Key	Equivalent Orders	Statement
А	Go to A Bar	Move the A-bar to the center of the waveform area; select A-bar by the cursor.
В	Go to B Bar	Move the B-bar to the center of the waveform area; select B-bar by the cursor.
Т	Go to T Bar	Move the T-bar to the center of the waveform area; select T-bar by the cursor.
E	Change to Zoom mode	Change the mouse mode to Zoom
н	Change to Hand mode	Change the mouse mode to Hand.

# 7.1 Hot Keys

## Table 7-2 : Hot Keys (2)

Hot Key	Equivalent Orders	Statement	
Ctrl + A	Go to A Bar	Center A-bar.	
Ctrl + B	Go to B Bar	Center B-bar.	
Ctrl + C	File -> Capture Window	Open Capture Graph dialog box.	
Ctrl + E	Data ->Zoom	Change Mouse mode to Zoom mode.	
Ctrl + F	Data -> Find Data Value	Search specific data with predetermined conditions.	
Ctrl + G	Bus/Signal -> Group into Bus	Group selected signals into a Bus.	
Ctrl + N	File -> New	Create a new file.	
Ctrl + O	File -> Open	Open a saved file.	
Ctrl + P	File -> Print	Print an active file.	
Ctrl + S	File-> Save	Save an active file with its current name, location and file format.	
Ctrl + U	Bus/Signal -> Ungroup from Bus	Ungroup signals (Pins) from a Bus.	
Ctrl + Z	Data -> Previous Zoom	Reverse the last zoom.	
Ctrl + Shift + E	File->Export Waveform	Open Export Waveform dialog box.	



## Table 7-3 : Hot Keys (3)

Hot Key	Equivalent Orders	Statement
Page Down	Operate the position shown	Go to next page of the data or the waveform
Page Up	Operate the position shown	Go to previous page of the data or the waveform
Home	Operate the position shown	Go to the beginning of the data or the waveform
End	Operate the position shown	Go to the end of the data or the waveform.
Up	Operate the position shown	Move the cursor up a grid.
Down	Operate the position shown	Move the cursor down a grid.
Left	Operate the position shown	Move the selected Bar or display left to prior the waveform or data.
Right	Operate the position shown	Move the selected Bar or display right to posterior the waveform or data.
ESC	Operate the position shown	Release all selected bars, and change Mouse mode to Normal.
Space	Change the trigger conditions	Change trigger conditions.

Table	7-4	: Hot	Keys	(4)
-------	-----	-------	------	-----

Hot Key	Equivalent Orders	Statement
F1	Help -> Logic Analyzer Help	Logic Analyzer Help
F2	Decrease the sampling rate	Decrease the sampling rate
F3	Increase the sampling rate	Increase sampling rate
F5	Run/Stop -> Single Run	Execute the acquirement once
F6	Run/Stop -> Repetitive Run	Execute the acquirement continuously
F7	Run/Stop -> Stop	Stop acquiring data
F8	Data -> Zoom Out	Zoom out the waveform
F9	Data -> Zoom In	Zoom in the waveform
F11	Data ->To the Previous Edge	Move forward to the prior variation waveform and center that location.
F12	Data -> To the Next Edge	Move forward to the next variation waveform and center that location.



# 7.2 Contact Us

#### Table 7-5: Contact Us

Contact Us			
Copyright 1997-2011, ZEROPLUS TECHNOLOGY CO., LTD			
Headquarter			
Taiwan- New Taipei City	ZEROPLUS TECHNOLOGY CO., LTD. 3F., No.121, Jian Ba Rd., Zhonghe Dist., New Taipei City, Taiwan Tel: +886-2-6620-2225 Fax: +886-2-6620-2226 ZIP Code: 23585		
<ul> <li>Instrument Division/ Business Department</li> </ul>			
Taiwan-Hsinchu City	ZEROPLUS TECHNOLOGY CO., LTD. 2F., No.242-1, Nanya St., North Dist., Hsinchu City 30052, Taiwan (R.O.C.) Tel: +886-3-542-6637 Ext.:87 Fax: +886-3-542-4917 ZIP Code: 30052 E-Mail: <u>Service_2@zeroplus.com.tw</u>		
Taiwan- New Taipei City	ZEROPLUS TECHNOLOGY CO., LTD. Address: 2F, NO.123, Jian Ba Rd, Zhonghe Dist., New Taipei City, Taiwan Tel: 886-2-6620-2225 Ext.:200 Fax: 886-2-6620-2226 Website: www.zeroplus.com.tw		
Other Service Departments			
China-Shenzhen	ZEROPLUS TECHNOLOGY (DONG GUAN) CO,. LTD. Room 2821, B2 Section, Building 1, Hong Rong Square, District 80, Bao'an, Shenzhen City, Guangdong Province, China Mainland Tel: +86-755-2955-6305~6 Fax: +86-755-2955-6306 #808 ZIP Code: 518102		
China-Shanghai	ZEROPLUS TECHNOLOGY (DONG GUAN) CO,. LTD. 101, No. 172, Alley 377, Chen Hui Road, Zhang Jiang, Pudong New Area, Shanghai City Tel: +86-21-50278005~6 Fax::+86-21-50278006 ZIP Code: 201203		

Users can download the newest Software and User Manual.

ZEROPLUS is the brand of ZEROPLUS TECHNOLOGY CO., LTD.

The other brands and products are the brand or registered trade mark of the individual company or organization.

# Conclusion

The demonstrations in this User Manual will enhance users' understanding of our products in future issues, even though the manual ends here. We thank you for choosing the Logic Analyzer. Please contact us if you find anything that could be done better, either in software or hardware. We appreciate your feedback.